XB6-P20A

Pulse counting module

User Manual

Nanjing Solidot Electronic Technology Co., Ltd.

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Nanjing Solidot Electronic Technology Co., Ltd.
Address: 11th Floor, Ang Ying Building, No. 91 Shengli Road, Jiangning District, Nanjing, Jiangsu Province
Zip code: 211106
Tel: 4007788929
Website:http://www.solidotech.com

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1 Product description

1.1 Product Introduction

XB6-P20A is a slice pulse counting module, which adopts X-bus bottom bus and can be connected to 24V single-ended encoders. The module supports Z-phase zero clearing, comparison output, probe latching and other functions. It can be widely used in various industrial system equipment when matched with our XB6 series coupler.

1.2 Product Features

- Three pulse modes
  Supports AB quadrature (ABZ), directional pulse (Pul+Dir), and double pulse (CW/CCW).
- Two ring counting ranges
  0~2^32-1 or 0~ring counting resolution × counting magnification-1.
- Speed reporting
  Supports reporting the real-time speed of two encoder channels.
- Z phase clear
  Support Z phase clear function.
- Comparison Output
  When the count value reaches the set value, the corresponding output channel outputs a pulse signal with adjustable time.
- Probe latch
  Supports latching the current count value when the voltage of the probe input pin changes.
- Magnification Count
  Supports 4x/2x/1x counting.
- Power-off storage
  Supports power-off storage of count values.
- Small volume
  Compact structure and small space occupation.
- Easy configuration
  The configuration is simple and supports mainstream PROFINET master and EtherCAT master.

- Easy to install
  DIN 35 mm standard rail installation
  It adopts spring-type terminal blocks, making wiring convenient and quick.

2 Product Parameters

2.1 General parameters

Interface parameters	
Product number	XB6-P20A
Bus protocol	X-bus
Process data volume: Downstream	20 Bytes
Process data volume: Uplink	34 Bytes
Channel Type	Encoder input channel: 2 groups of channels (Phase A, Phase B, and Phase Z), PNP/NPN
	Probe input channels: 4 channels (1 encoder with 2 probe functions), PNP/NPN
	Ordinary digital input channel: 4 channels（1 encoder with 2 normal Digital quantity enter), PNP/NPN
	Comparison output channels: 4 channels (1 encoder with 2 comparison outputs), NPN
	Ordinary digital output channel: 4 channels（1 encoder with 2 normal Digital output), NPN
Refresh rate	1 ms

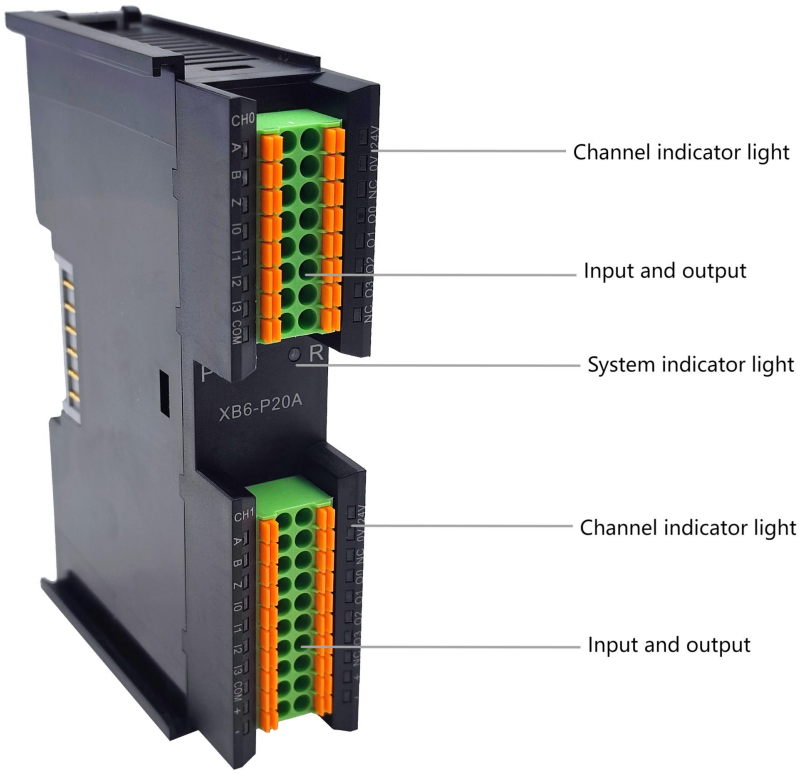
Technical Parameters	
System input power	5VDC
Field side power supply rating (range)	24VDC (18V~36V)
Input channel voltage rating (range)	24VDC (15V~30V)
Encoder pulse input mode	AB quadrature (ABZ), directional pulse (Pul+Dir), double pulse (CW/CCW)
Encoder pulse input frequency	1MHz
Report channel real-time speed	Support
Z phase clear	Support
Counting rate setting	4x/2x/1x (default 1x)
Ring counting	Support
Counting range	0~2^32-1 or0~Ring counting resolution × counting magnification - 1
Encoder ring count resolution setting[1]	Support (Ring count resolution setting range is 0~65535)
Count initial value setting	Support (the initial value of the count is set in the range of 0~2^32-1)
Count backwards	Support
Encoder input hardware filtering	Support (0~15 levels)
Probe function (high-speed hardware latch)	Support
Probe input frequency	1MHz
Comparison output function	Support
Compare output signal response speed	50us
Input and output pin function selection	Support
Power-off storage	Support
Dimensions	106×73×25.7mm
Weight	105g
Wiring	Screw-free quick plug
Installation	35mm rail installation
Operating temperature	-10℃~+60℃
Storage temperature	-20℃~+75℃
Relative humidity	95%, non-condensing
Protection level	IP20

Note [1]: The ring count resolution here is only used to set the ring count range of the encoder and is different from the physical resolution of the encoder itself.

3 Panel

3.1 Module Structure

Product Parts Name



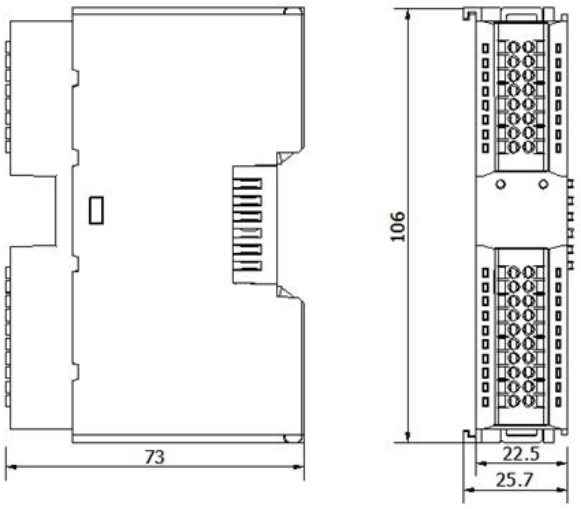
3.2 Indicator light function

Name	Logo	Color	State	Status description
Power Indicator	P	Green	Always on	Power supply is normal
			Off	The product is not powered on or the power supply is abnormal
Communication indicator	R	Green	Always on	The system is running normally
			Flashing 1Hz	The module is connected and the X-bus system is ready to interact
			Off	The device is not powered on, the X-bus is not exchanging data, or an exception occurs.
Encoder input AB phase indicator	A	Green	Always on	Encoder enabled
	B		Off	Encoder not enabled
Encoder input Z phase indicator	Z	Green	Always on	The encoder Z phase clear function has been enabled
			Off	The encoder Z phase clear function is not enabled
Input channel indicator	I0~I3	Green	Always on	Channel has signal input
			Off	Channel no signal input
Output channel indicator	O0~O3	Green	Always on	Channel has signal output
			Off	Channel no signal output

4 Installation and removal

4.1 Dimensions

Dimensions (unit: mm)



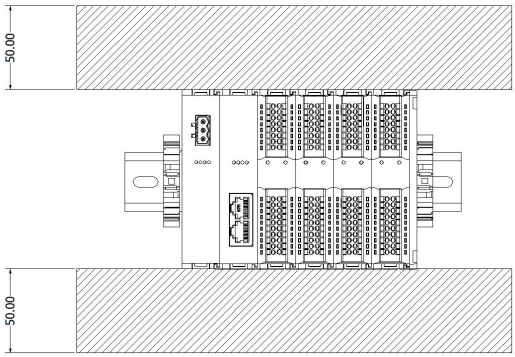
4.2 Installation Guide

Installation\removal precautions

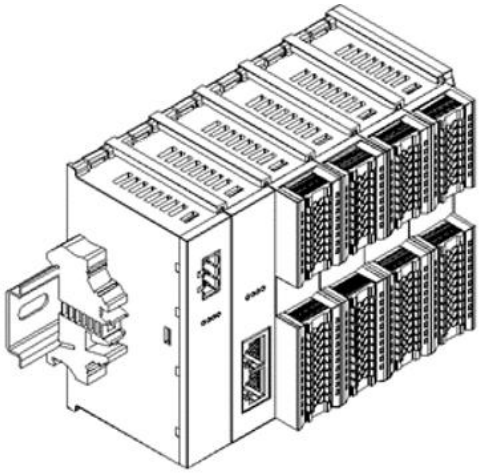
- Ensure that the cabinet has good ventilation measures (such as installing an exhaust fan in the cabinet).
- Do not install this device near or over any equipment that may cause overheating.
- Be sure to install the module vertically and maintain air circulation around it (there should be at least 50 mm of air circulation space above and below the module).

- After the module is installed, be sure to install the guide rail fixings at both ends to secure the module.
- Installation and removal must be performed with the power turned off.

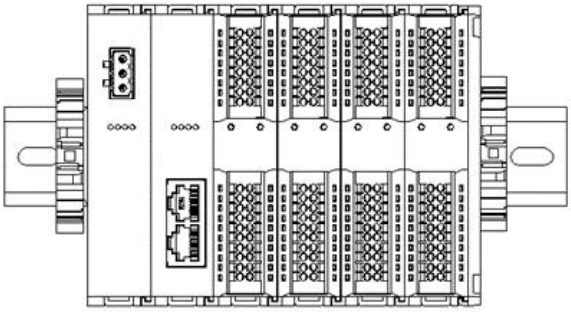
Minimum gap for module installation (≥50mm)



Ensure the module is installed vertically



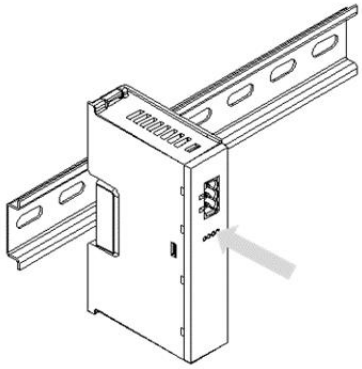
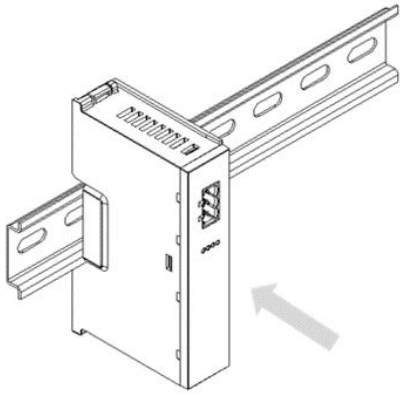
Be sure to install the rail fixings



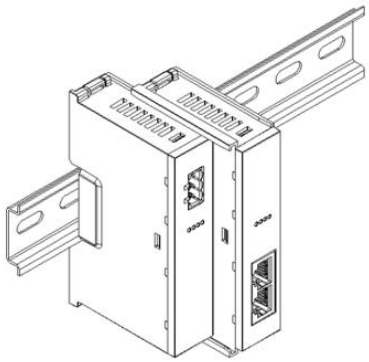
4.3 Installation and removal steps

Module installation and removal	
Module installation steps	1. Install the power module on the fixed rail first.
	2. Install the coupler and required I/O modules in sequence on the right side of the power module.
	3. After installing all required I/O modules, install the end cover to complete the module assembly.
	4. Install the guide rail fixings at both ends of the power module and end cover to fix the module.
Module disassembly steps	1. Loosen the guide rail fixings at both ends of the module.
	2. Use a flat-blade screwdriver to pry open the module buckle.
	3. Pull out the disassembled module.

4.4 Installation diagram

Power module installation	**Step**
 ①	Insert the power module guide slot and align it vertically with the guide rail as shown in the left figure ①.
 ②	As shown in the left figure ②, press the power module hard until you hear a "click" sound, and the module is installed in place.

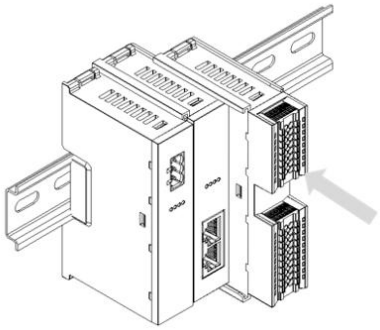
Coupler module installation	Step



③

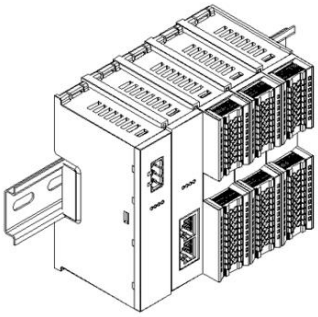
Align the left slot of the coupler module with the right side of the power module and push it in as shown in ③ in the left figure.
Press the power module firmly until you hear a "click" sound and the module is installed in place.

I/O Module Installation	Step



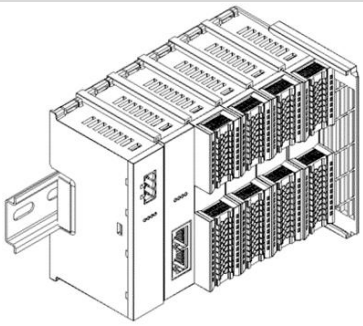
④

Follow the steps of installing the coupler module in the previous step and install the required I/O modules one by one, as shown in Figure ④ and Figure ⑤ on the left.



⑤

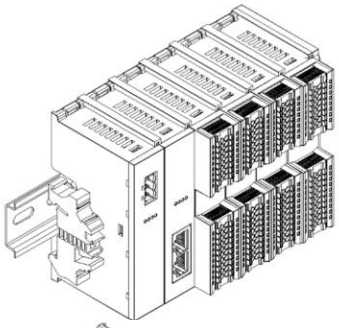
End cap installation	Step



⑥

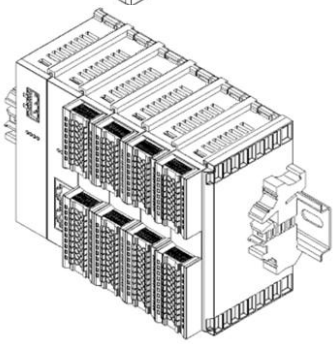
Install the end cover on the right side of the last module, as shown in Figure ⑥ on the left. For installation methods, refer to the installation method of the coupler module.

Rail fixing installation	Step



⑦

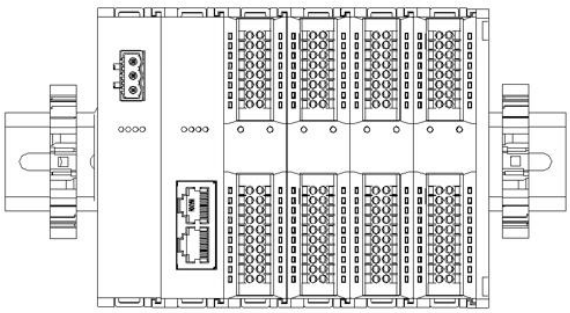
Install and lock the guide rail fixings close to the left side of the coupler, as shown in Figure ⑦ on the left.



⑧

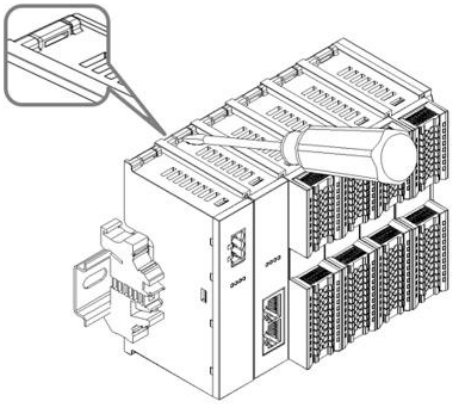
Install the guide rail fixture on the right side of the end cover. First push the guide rail fixture towards the coupler to ensure that the module is installed firmly, and then use a screwdriver to tighten the guide rail fixture, as shown in the left figure ⑧.

Disassembly	Step

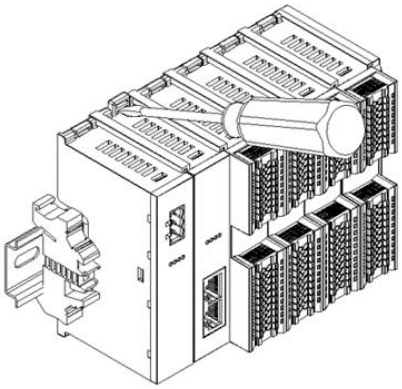


⑨

Use a screwdriver to loosen the guide rail fixing at one end of the module and move it to one side to ensure that there is a gap between the module and the guide rail fixing, as shown in Figure ⑨ on the left.



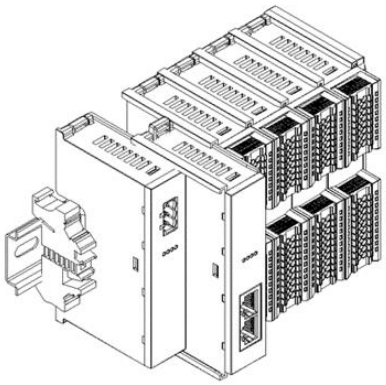
⑩



⑪

Insert a flat-head screwdriver into the buckle of the module to be removed, and apply force to the module sideways (until you hear a sound), as shown in the left figure ⑩ and⑪shown.

Note: Each module has a buckle on the top and bottom, and the same method should be used for all modules.

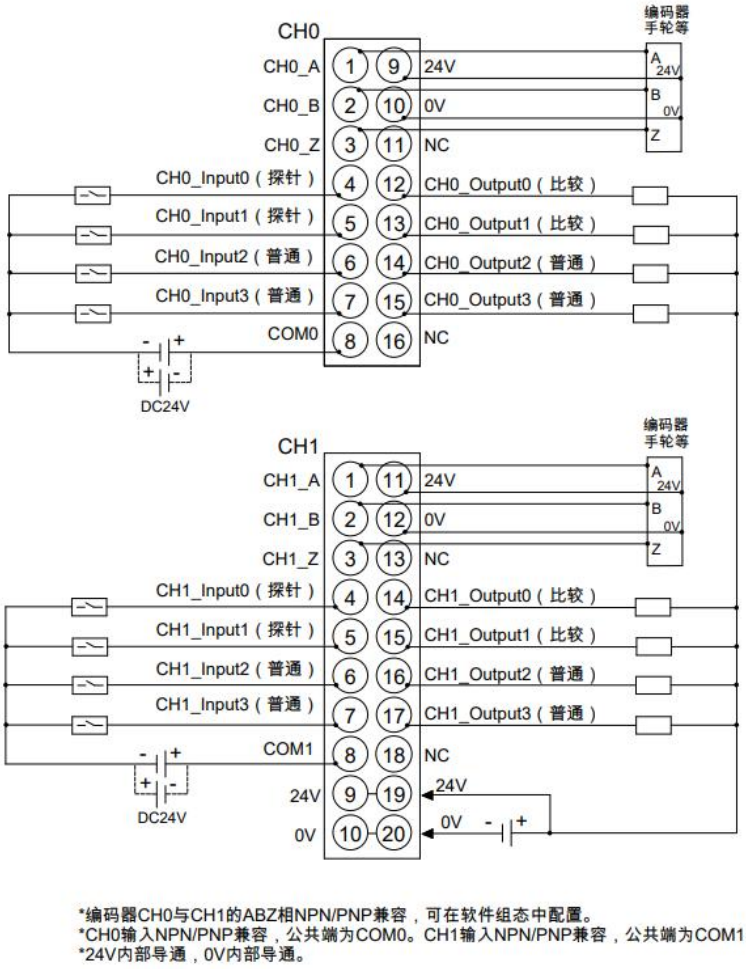


⑫

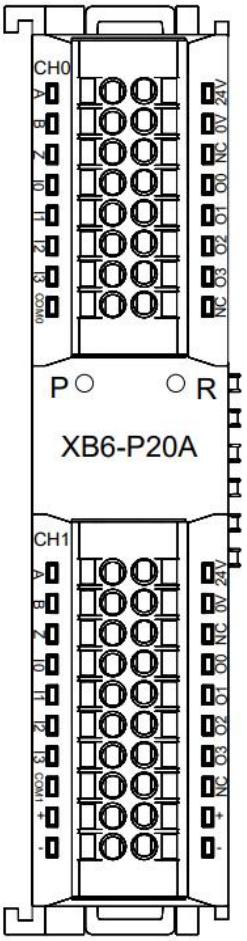
Follow the opposite operation of installing the module to remove the module, as shown in the left figure⑫Shown.

5 Wiring

5.1 Wiring Diagram



*编码器CH0与CH1的ABZ相NPN/PNP兼容，可在软件组态中配置。
*CH0输入NPN/PNP兼容，公共端为COM0。CH1输入NPN/PNP兼容，公共端为COM1。
*24V内部导通，0V内部导通。



- For personal and equipment safety, it is recommended to disconnect the power supply when performing wiring operations.

5.2 Terminal Block Definition

CH0					
Terminal number	**Terminal marking**	**Illustrate**	**Terminal number**	**Terminal marking**	**Illustrate**
1	A	CH0_A	9	24V	24V encoder power supply
2	B	CH0_B	10	0V	0V encoder power supply
3	Z	CH0_Z	11	NC	Empty terminal
4	I0	CH0_Input1 (probe function)	12	O0	CH0_Output1 (Comparison Output)
5	I1	CH0_Input2 (probe function)	13	O1	CH0_Output2 (Comparison Output)
6	I2	CH0_Input3 normal DI	14	O2	CH0_Output3 normal DO
7	I3	CH0_Input4 normal DI	15	O3	CH0_Output4 normal DO
8	COM	Input common 1	16	NC	Empty terminal
CH1					
Terminal number	**Terminal marking**	**Illustrate**	**Terminal number**	**Terminal marking**	**Illustrate**
1	A	CH1_A	11	24V	24V encoder power supply
2	B	CH1_B	12	0V	0V encoder power supply
3	Z	CH1_Z	13	NC	Empty terminal
4	I0	CH1_Input1 (Probe function)	14	O0	CH1_Output1 (Comparison Output)
5	I1	CH1_Input2 (Probe function)	15	O1	CH1_Output2 (Comparison Output)
6	I2	CH1_Input3 Normal DI	16	O2	CH1_Output3 normal DO
7	I3	CH1_Input4 Normal DI	17	O3	CH1_Output4 normal DO
8	COM	Input common 2	18	NC	Empty terminal
9	+	Power+	19	+	Power+
10	-	power supply-	20	-	power supply-

6 Use

6.1 Process data

6.1.1 Uplink data

Uplink data 34 bytes (17 bytes for each encoder, encoder [n] value is 1~2)				
name	**meaning**	**Ranges**	**type of data**	**length**
Encoder_[n] Probe Input CH1	Encoder probe input signal channel 1	0: No signal input 1: There is signal input	bool	1 person
Encoder_[n] Probe Input CH2	Encoder probe input signal channel 2	0: No signal input 1: There is signal input	bool	1 person
Encoder_[n] Input CH3	Encoder common input signal channel 3	0: No signal input 1: There is signal input	bool	1 person
Encoder_[n] Input CH4	Encoder common input signal channel 4	0: No signal input 1: There is signal input	bool	1 person
Encoder_[n] Probe Input CH1 Latched Finish	Encoder probe input channel 1 latch completion flag	0: 1->0 latched once, flipped once 1: 0->1 latch once, flip once	bool	1 person
Encoder_[n] Probe Input CH2 Latched Finish	Encoder probe input channel 2 latch completion flag	0: 1->0 latched once, flipped once 1: 0->1 latch once, flip once	bool	1 person
Encoder_[n] Count Value	Encoder count	0~2^32-1	unsigned32	4 bytes

	value			
Encoder_[n] Latch CH1 Value	Encoder probe input channel 1 latch value	0~2^32-1	unsigned32	4 bytes
Encoder_[n] Latch CH2 Value	Encoder probe input channel 2 latch value	0~2^32-1	unsigned32	4 bytes
Encoder_[n] Speed	Encoder speed	-2^31~2^31-1	signed32	4 bytes

Uplink data description:

- **Encoder probe input signal channel Encoder_[n] Probe Input CH1/CH2**
  Each encoder is equipped with 2 probe input channels, indicating the presence or absence of input signals from the corresponding probe input channels.
  When the probe input channel latch function is not enabled, it can be used as a normal digital input channel.

- **Encoder common input signal channel Encoder_[n] Input CH3/CH4**
  Each encoder is equipped with 2 ordinary digital input channels, indicating the presence or absence of the corresponding DI channel input signal.

- **Encoder probe input channel latched completion flag Encoder_[n] Probe Input CH1/CH2 Latched Finish**
  One encoder is equipped with two probe input channels. After the probe input channel completes a latch, the flag bit will flip from 0->1 or 1->0.
  Example 1: The latch completion flag of encoder 1 probe input channel 1 is 0. After completing one latch, the flag becomes 1. After completing another latch, the flag becomes 0.

- **Encoder count value Encoder_[n] Count Value**
  The encoder count value corresponds to the current count value of the encoder, and the value range is 0~2^32-1.

- **Encoder probe input channel latch value Encoder_[n] Latch CH1/CH2 Value**
  Each encoder is equipped with 2 probe input channels. By inputting a signal that meets the set conditions into the probe input channel, the current count value of the corresponding encoder can be quickly latched. Therefore, the value range of the latched value is the same as the count value, which is 0~2^32-1.

- **Encoder speed Encoder_[n] Speed**
  The encoder speed is the pulse speed of the encoder input channel, and its value range is -2^31~2^31-1.

6.1.2 Downlink data

Downlink command 20 bytes (10 bytes for each encoder, encoder [n] value 1~2)				
name	**meaning**	**Ranges**	**type of data**	**length**
Encoder_[n] Enable	Encoder count enable	0: Incapacity 1: Enable	bool	1 bit bit0
Encoder_[n] Z Phase Clear Enable	Encoder Z phase clear enable	0: Incapacity 1: Enable	bool	1 bit bit1
Encoder_[n] Count Clear	Encoder count value cleared	0: Incapacity 1: Enable	bool	1 bit bit2
Encoder_[n] Compare Output CH1 Enable	Encoder comparison output channel 1 enable	0: Incapacity 1: Enable	bool	1 bit bit3
Encoder_[n] Compare Output CH2 Enable	Encoder comparison output channel 2 enable	0: Incapacity 1: Enable	bool	1 bit bit4
Encoder_[n] Compare Output CH1 Direction	Encoder comparison output channel 1 comparison direction	0: Decrement comparison 1: Incremental comparison	bool	1 bit bit5
Encoder_[n] Compare Output CH2 Direction	Encoder comparison output channel 2 comparison direction	0: Decrement comparison 1: Incremental comparison	bool	1 bit bit6
Encoder_[n] Compare Output CH1 Mode	Encoder comparison output channel 1 trigger mode	0: Single trigger 1: Repeated trigger	bool	1 bit bit7
Encoder_[n] Compare Output CH2 Mode	Encoder comparison output channel 2 trigger mode	0: Single trigger 1: Repeated trigger	bool	1 bit bit0
Encoder_[n] Output CH1(Compare)	Encoder output channel 1 (comparison output)	0: Output high level 24V 1: Output low level 0V	bool	1 bit bit1
Encoder_[n] Output CH2(Compare)	Encoder output channel 2 (comparison output)	0: Output high level 24V 1: Output low level 0V	bool	1 bit bit2
Encoder_[n] Output CH3	Encoder output channel 3 (normal output)	0: Output high level 24V 1: Output low level 0V	bool	1 bit bit3
Encoder_[n] Output	Encoder output channel 4	0: Output high	bool	1 bit bit4

CH4	(normal output)	level 24V 1: Output low level 0V		
Encoder_[n] Input Latch CH1 Enable	Encoder probe input channel 1 latch enable	0: Incapacity 1: Enable	bool	1 bit bit5
Encoder_[n] Input Latch CH2 Enable	Encoder probe input channel 2 latch enable	0: Incapacity 1: Enable	bool	1 bit bit6
Encoder_[n] Compare Output CH1 SetValue	Encoder comparison output channel 1 setting value	0~2^32-1	unsigned32	4 bytes
Encoder_[n] Compare Output CH2 SetValue	Encoder comparison output channel 2 set value	0~2^32-1	unsigned32	4 bytes

Downlink data description:

- **Encoder count enable Encoder_[n] Enable**
  The encoder count enable is set to 0 to disable and set to 1 to enable.

- **Encoder Z Phase Clear Enable Encoder_[n] Z Phase Clear Enable**
  If the encoder Z phase clear enable is set to 0, it is disabled, and if it is set to 1, it is enabled.
  After the Z-phase clear is enabled, the current count value is cleared by detecting the Z-phase signal of the encoder. Each time the encoder rotates one circle, a Z-phase pulse is generated and the count value is cleared once.
  The physical resolution of the encoder is the number of pulses output by the encoder when it rotates one circle. The counting ratio × physical resolution is the maximum value of the single-circle count. When the Z-phase clear function is turned on and the count value increases or decreases, the count value is cleared once every time the encoder rotates one circle.

- **Encoder count value clear Encoder_[n] Count Clear**
  Edge control, when it is detected that this bit is set from 0 to 1, the corresponding encoder count value is cleared. If the encoder count initial value is set, the count value is also set to 0.

- **Encoder Compare Output -- Channel Enable Encoder_[n] Compare Output CH1/CH2 Enable**
  The encoder comparison output enable is set to 0 to disable and set to 1 to enable.
  When the comparison output channel function is not enabled, it can be used as a normal digital output channel.
  See6.2.3 Comparison output function.

- **Encoder Compare Output - Channel Compare Direction Encoder_[n] Compare Output CH1/CH2 Direction**
  The comparison direction of the encoder comparison output channel is set to 0 for decremental comparison, that is, the count value is from large to small; it is set to 1 for increment comparison, that is, the count value is from small to large.

- **Encoder Compare Output -- Channel Trigger Mode Encoder_[n] Compare Output CH1/CH2 Mode**
  Encoder comparison output channel trigger mode can beSet to: 0 (single trigger), 1 (repeated trigger).
  After the single trigger comparison output function is enabled, a pulse output is triggered when the count value meets the condition, and no comparison is made afterwards. To trigger the comparison output again, the comparison output function needs to be enabled again.
  After the repeated triggering comparison output function is enabled, a pulse output is triggered when the count value meets the condition, and then the next comparison will start immediately, but the pulse output will not be restarted again within the comparison output pulse time. After the comparison output triggers the pulse for a period of time, the pulse output will be triggered again if the comparison output condition is met.6.2.3 Comparison output function.

- **Encoder output channel (Compare output) Encoder_[n] Output CH1/CH2 (Compare)**
  When the comparison output channel function is not enabled, it can be used as a common digital output channel. Digital channel output (NPN type output): set to "0" to output high level 24V, set to "1" to output low level 0V.
  When the comparison output is established, the level of this pin will be flipped, so you can set the invalid/valid level corresponding to the comparison output by setting this bit first and then enabling the comparison output.

- **Encoder output channel (normal output) Encoder_[n] Output CH3/CH4**
  Digital channel output (NPN type output): Set to "0" to output high level 24V, set to "1" to output low level 0V.

- **Encoder probe input channel latch enable Encoder_[n] Input Latch CH1/CH2 Enable**
  If the encoder input latch channel enable flag is set to 1, the latch function is enabled; if it is set to 0, the latch function is disabled.
- **Encoder comparison output channel set value Encoder_[n] Compare Output CH1/CH2 SetValue**
  The encoder comparison output channel setting value is consistent with the encoder counting range, which is 0~2^32-1.
  After the comparison output function is enabled, the module will compare the current count value with the set value to see if they are consistent. When the comparison direction is consistent with the comparison set value, the corresponding comparison output channel will output a pulse with adjustable time.. See6.2.3 Comparison output function.

6.2 Configuration parameter definition

The module configuration has a total of 24 parameters. The two encoders have 11 identical configuration parameters that are configured independently, and 2 configuration parameters are shared by the two encoders (the shared parameters are marked in green in the table below). Encoder 1 is used as an example to introduce the configuration parameters, as shown in the table below. Note: The configuration parameters will take effect the next time the encoder is enabled.

Function	parameter name	Ranges	default value
Encoder 1 pulse mode	Encoder1 Pulse Mode	0: ABZ (AB orthogonal)	0
		1: Pul+Dir (direction pulse)	
		2: CW/CCW (double pulse)	
Encoder 1 Filter	Encoder1 Filter	Level 0~15	7
Encoder 1 counting rate	Encoder1 Count Multiples	1, 2, 4 (valid only in AB orthogonal mode)	1
Encoder 1 counting range	Encoder1 Count Range	0: 2^32 (0~2^32-1)	0
		1: Resolution × Multiples (0~Ring counting resolution× counting magnification-1, only valid in AB orthogonal mode)	
Encoder 1 ring count resolution	Encoder1 Count Resolution	0~65535	0
Encoder 1 counting direction	Encoder1 Count Direction	0: Forward	0
		1: Reverse	
Encoder 1 count initial value	Encoder1 Count Initial Value	0~2^32-1	0
Encoder 1 Probe Mode	Encoder1 Probe Trigger Mode	0: CH1_Single CH2_Single Channel 1 single, channel 2 single	0
		1: CH1_Repeat CH2_Single Channel 1 repeat, channel 2 single	
		2: CH1_Single CH2_ Repeat Channel 1 single, channel 2 repeat	
		3: CH1_ Repeat CH2_ Repeat Channel 1 repeat, channel 2 repeat	
Encoder 1 probe trigger edge	Encoder1 Probe Trigger Edge	0: CH1_Raising CH2_Raising Channel 1 rising edge, channel 2 rising edge	0
		1: CH1_Falling CH2_Raising Channel 1 falling edge, channel 2 rising edge	

		2: CH1_Raising CH2_Falling Channel 1 rising edge, channel 2 falling edge	
		3: CH1_Falling CH2_Falling Channel 1 falling edge, channel 2 falling edge	
Encoder 1 comparison output channel 1 pulse time	Encoder1 Compare Output CH1 Time	0~65535 (unit: ms)	10
Encoder 1 comparison output channel 2 pulse time	Encoder1 Compare Output CH2 Time	0~65535 (unit: ms)	10
Power-off storage enable	Power Down Storage	0: OFF	1
		1: ON	
Encoder NPN/PNP signal setting	Encoder Signal Type	0: NPN	0
		1: PNP	

6.2.1 Encoder counting function

The encoder counting parameters include 7 parameters: encoder pulse mode, filtering, counting ratio, counting range, ring counting resolution, counting direction and counting initial value.

Encoder pulse mode: The input pulse modes supported by the encoder count include AB quadrature mode, direction pulse mode and CW/CCW mode.

Encoder filtering: The encoder filter is effective in all three pulse modes. There are 16 levels of filtering (0~15), with level 0 indicating no filtering and level 15 indicating the maximum filtering. The encoder filter parameter defaults to level 7 and can be configured as needed.

Encoder counting ratio: The encoder count multiplier is only effective in AB quadrature pulse mode.

Encoder counting range: The encoder's counting range can be set to 0~2^32-1 or 0~ring counting resolution × counting ratio-1. The former is suitable for most cases, and the latter is suitable for situations where the encoder has no Z-phase signal but still needs to be used for single-turn counting.

Encoder ring count resolution: The ring counting resolution is used to set the counting range of the encoder, and the setting range is 0~65535.

Note: The ring count resolution here is different from the physical resolution of the encoder itself.

Encoder counting direction: The encoder counting direction defaults to 0, which is forward counting; when it is set to 1, the encoder will count in the reverse direction after the encoder is re-enabled.

Encoder count initial value: The encoder count initial value supports configuration and automatically takes effect after the encoder is re-enabled. The setting range of the count initial value is 0~2^32-1. Note: When the power-off storage function is enabled, the count initial value is invalid and the encoder count initial value is 0.

example 1: The encoder 1 pulse mode is set to AB quadrature mode, the encoder count range is selected to be 0~ring count resolution × count magnification - 1, the ring count resolution is set to 50000, the count magnification is 4, the count direction is forward, the initial count value is 0, and the count range is 0~200000. The module is connected to an encoder with a physical resolution of 1000. After counting starts, the count value starts to increase from 0. The encoder rotates one circle and the count value is 1000×4 = 4000. After reaching 200000, it returns to 0 and continues counting.

6.2.2 Probe function

The probe function parameters include probe mode and probe trigger edge. Each encoder is equipped with 2 probe input channels. By inputting corresponding signals to the probe input channels, the count value of the corresponding encoder can be latched.

Probe Mode: The probe mode parameter can configure each probe function channel of the encoder to single/continuous mode.

If the probe function channel is configured in single-shot mode, after the probe function is enabled, when the channel inputs a signal that meets the set conditions, the count value can be latched once; when a signal that meets the set conditions is input again subsequently, the count value will no longer be latched unless the probe function channel is re-enabled.

If the probe function channel is configured in continuous mode, after the probe function is enabled, each time the channel inputs a signal that meets the set conditions, the count value can be latched once, and the count value can be latched multiple times.

Probe trigger edge: Each probe function channel of the encoder can be configured as rising edge/falling edge trigger through the probe trigger edge parameter. The latch trigger signal of the two probe function channels of each encoder can be configured separately, and the latch value can be displayed separately.

The probe input channel is compatible with PNP/NPN signals through the COM terminal. When the COM terminal is connected to 0V, the input signal is PNP type, the input high level 24V signal is valid, and the input low level 0V signal is invalid; when the COM terminal is connected to 24V, the input signal is NPN type, the input low level 0V signal is valid, and the input high level 24V signal is invalid.

Rising edge triggering means that the probe input channel is triggered from an invalid signal to a valid signal, and falling edge triggering means that it is triggered from a valid signal to an invalid signal.

6.2.3 Comparison output function

Comparison output function By configuring the comparison output channel enable, comparison output set value, comparison direction, single/repeated trigger mode and comparison output channel pulse time, when the encoder count value reaches the set value and meets the comparison direction, the corresponding comparison output channel will output a time-adjustable pulse, and the adjustable time is the comparison output pulse time. The pulse output response speed of the comparison output function can reach 50us level.

The configuration parameters of the comparison output function include the encoder comparison output channel pulse time, and the configurable time range is 0~65535ms.

Each encoder is equipped with 2 comparison output channels. The comparison output channel enable, comparison output set value, comparison direction and single/repeat trigger mode can all be set in the downlink data. When the comparison output channel function is not enabled, the comparison output channel can be used as a normal digital output.

Example 1: When the comparison output channel 1 of encoder 1 is used as a normal digital output, the output value is set to 0 (NPN type output, the output is 24V), the channel indicator light is off.

The setting value of encoder 1 comparison output channel 1 is set to 1000, the comparison direction is set to incremental comparison, the comparison output trigger mode is single trigger, and the comparison output channel 1 pulse time is configured to 5s. After the comparison output channel 1 function is enabled, when the count value of encoder 1 reaches 1000 from small to large (satisfying the comparison direction), comparison output channel 1 will be used as the comparison output channel output, and the state will be reversed from the original high-level output to low-level output. The pulse output time is 5s, and the channel indicator will be on for 5s. After 5s, the high-level output is restored and the channel indicator goes out. When the count value meets the comparison output setting value and comparison direction again, since the comparison output trigger mode is single trigger, the comparison output channel has no response.

Example 2: When the comparison output channel 1 of encoder 1 is used as a normal digital output, the output value is set to 1 (NPN type output, the output is 0V at this time), the channel indicator light is always on.

The setting value of encoder 1 comparison output channel 1 is set to 1000, the comparison direction is set to decrement comparison, the comparison output trigger mode is repeated trigger, and the comparison output channel 1 pulse time is configured to 5s. After the comparison output channel 1 function is enabled, when the count value of encoder 1 reaches 1000 from small to large (not meeting the comparison direction), the comparison output channel 1 has no response; when the count value of encoder 1 reaches 1000 from large to small (meeting the comparison direction), the comparison output channel will be used as the comparison output channel output, and the state will be reversed from the original low-level output to high-level output. The pulse output time is 5s, and the channel indicator light will go out for 5s. After 5s, the low-level output will be restored, and the channel indicator light will be always on.

The comparison output trigger mode is repeated triggering. When the count value meets the comparison output setting value and comparison direction again within the pulse output time of 5s, the comparison output channel will not change the pulse output state and continue to complete the 5s pulse

output. When the comparison condition is met again after 5s, the state will be reversed again, from the original high-level output to low-level output, the pulse output time is 5s, and the channel indicator light will go out for 5s. The comparison output repeated triggering is similar.

6.2.4 Power-off storage function

When the power-off storage enable parameter is turned on, the encoder count value can be stored when the system is powered off. The default value is 1, which means the power-off storage function is turned on, and the default value is 0, which means the power-off storage function is turned off.

When the power-off storage function is enabled, the encoder count initial value is invalid and the encoder count initial value is 0.

6.2.5 Encoder NPN/PNP signal setting

The A-phase, B-phase and Z-phase input channels of the two encoders are compatible with NPN/PNP signals. The encoder signal defaults to 0 for NPN signal and 1 for PNP signal.

6.3 Use Cases

- **Encoder 1 inputs AB quadrature pulses, the number of pulses is 40,000, and encoder 1 probe input channel 1 is latched**
  a. Configure the configuration parameters;
     a) The encoder 1 pulse mode is set to AB quadrature pulse mode, that is, Encoder1 Pulse Mode is set to 0: ABZ;
     b) The encoder 1 count multiple is set to 4 times, that is, Encoder1 Count Multiples is set to 4;
     c) The encoder 1 count range is set to 0~ring count resolution×count multiples-1, that is, Encoder1 Count Range is set to 1: Resolution×Multiples;
     d) The encoder 1 ring count resolution is set to 20000, that is, Encoder1 Count Resolution is set to 20000;
     e) The encoder 1 counting direction is set to forward counting, that is, Encoder1 Count Direction is set to 0: Forward;
     f) The initial value of encoder 1 count is set to 0, that is, Encoder1 Count Initial Value is set to 0;
     g) The probe mode of encoder 1 is set to single for channel 1 and single for channel 2, that is, Encoder1 Probe Trigger Mode is set to 0: CH1_Single CH2_Single;
     h) The encoder 1 probe trigger edge is set to the rising edge of channel 1 and the rising edge of channel 2, that is, Encoder1 Probe Trigger Edge is set to 0: CH1_Raising CH2_Raising;
  b. Set encoder 1 counting enable and encoder 1 probe input channel 1 latch enable;
     a) Downlink data Encoder_1 Enable is set to 1;
     b) Downlink data Encoder_1 Input Latch CH1 Enable is set to 1;
  c. Encoder 1 starts inputting pulses, and encoder 1 probe input channel 1 inputs valid signals.
- **Encoder 1 input direction pulse, pulse quantity 40000, encoder 1 comparison output channel 1 comparison output**
  a. Configure the configuration parameters;
     a) The encoder 1 pulse mode is set to the direction pulse mode, that is, Encoder1 Pulse Mode is set to 1: Pul+Dir;
     b) The encoder 1 count range is set to 0~2^32-1, that is, Encoder1 Count Range is set to 0:2^32;
     c) The encoder 1 counting direction is set to forward counting, that is, Encoder1 Count Direction is set to 0: Forward;
     d) The initial value of encoder 1 count is set to 0, that is, Encoder1 Count Initial Value is set to 0;
     e) The encoder 1 compare output channel 1 pulse time is set to 10s, that is, Encoder1 Compare Output CH1 Time is set to 10000;
  b. Set encoder 1 counting enable, encoder 1 comparison output channel 1 set comparison set value, comparison direction and comparison mode and enable;
     a) Downlink data Encoder_1 Enable is set to 1;
     b) Downlink data Encoder_1 Compare Output CH1 Set Value is set to 1000;
     c) Downlink data Encoder_1 Compare Output CH1 Direction is set to 1 for incremental comparison;
     d) Downlink data Encoder_1 Compare Output CH1 Mode is set to 1 Repeat Trigger;
     e) Downlink data Encoder_1 Compare Output CH1 Enable is set to 1 to enable;
  c. Encoder 1 starts inputting pulses.

6.4 Module Configuration Description

6.4.1 Application in TwinCAT3 software environment

1、Preparation

- **Hardware Environment**
  - **Module model XB6-P20A**
  - **Power module, EtherCAT coupler, end cap**

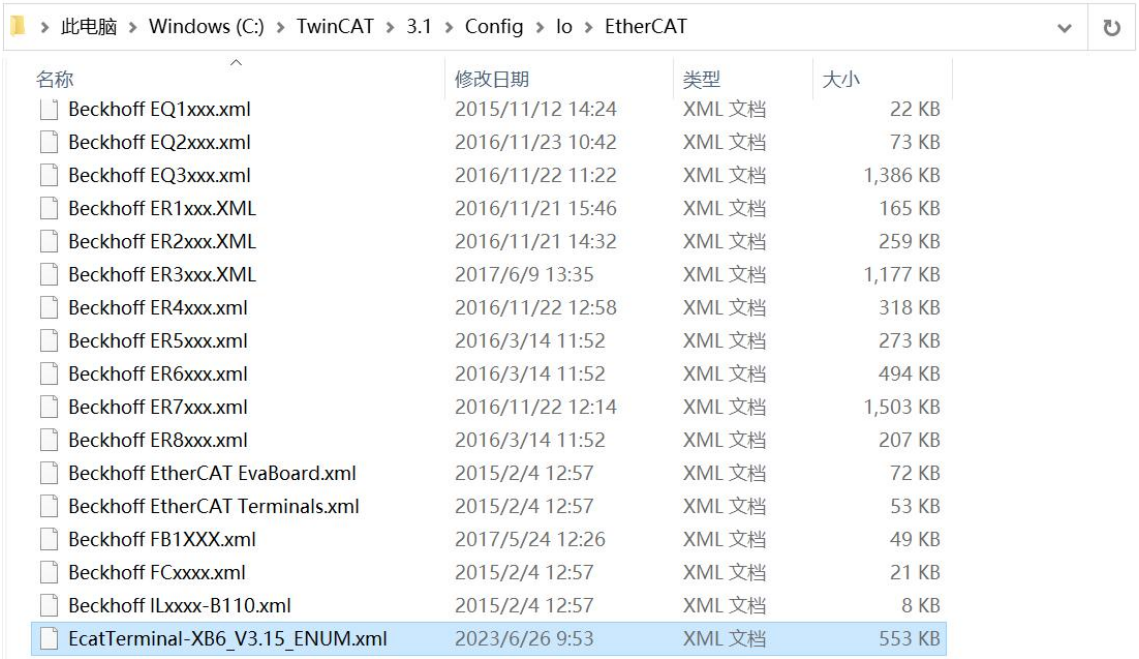
  This description takes XB6-P2000H power supply and XB6-EC0002 coupler as an example
  - **A computer with TwinCAT3 software pre-installed**
  - **EtherCAT dedicated shielded cable**
  - **Pulse output type sensor and other equipment, this description takes the connection of XB6-P04A module as an example**
  - **Encoder and other equipment**
  - **Switching power supply**
  - **Module mounting rails and rail fixings**
  - **Device Profile**

    Configuration file acquisition address:https://www.solidotech.com/documents/configfile
- **Hardware configuration and wiring**

  Please follow"4 Installation and removal""5 WiringRequest action

2、Pre-configured configuration files

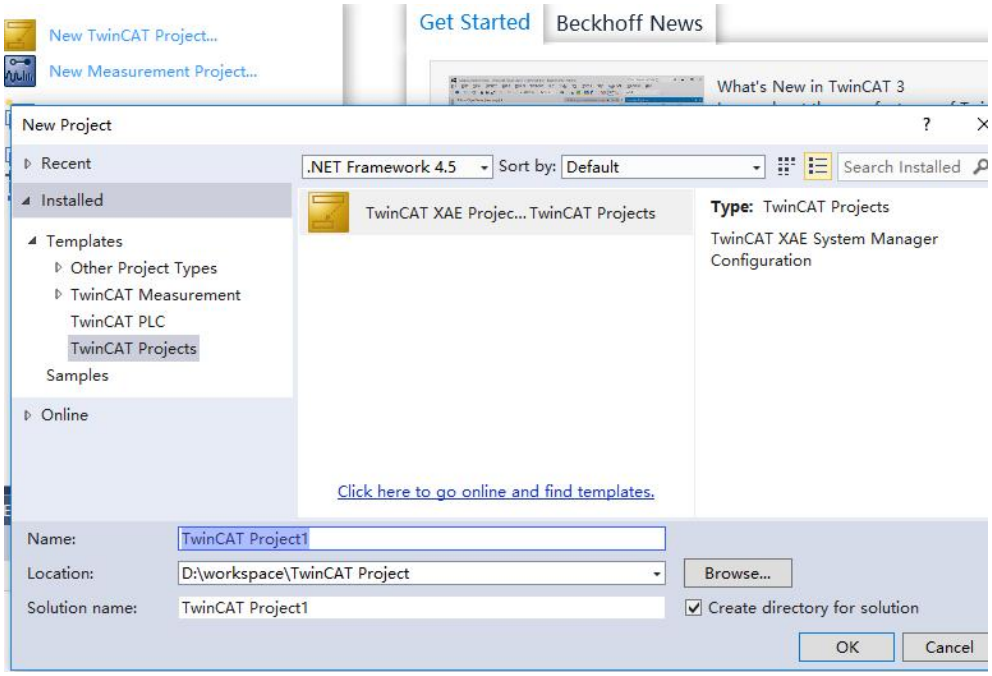
Place the ESI configuration file (EcatTerminal-XB6_V3.15_ENUM.xml) in the TwinCAT installation directory "C:\TwinCAT\3.1\Config\Io\EtherCAT", as shown in the figure below.



3、Create a project

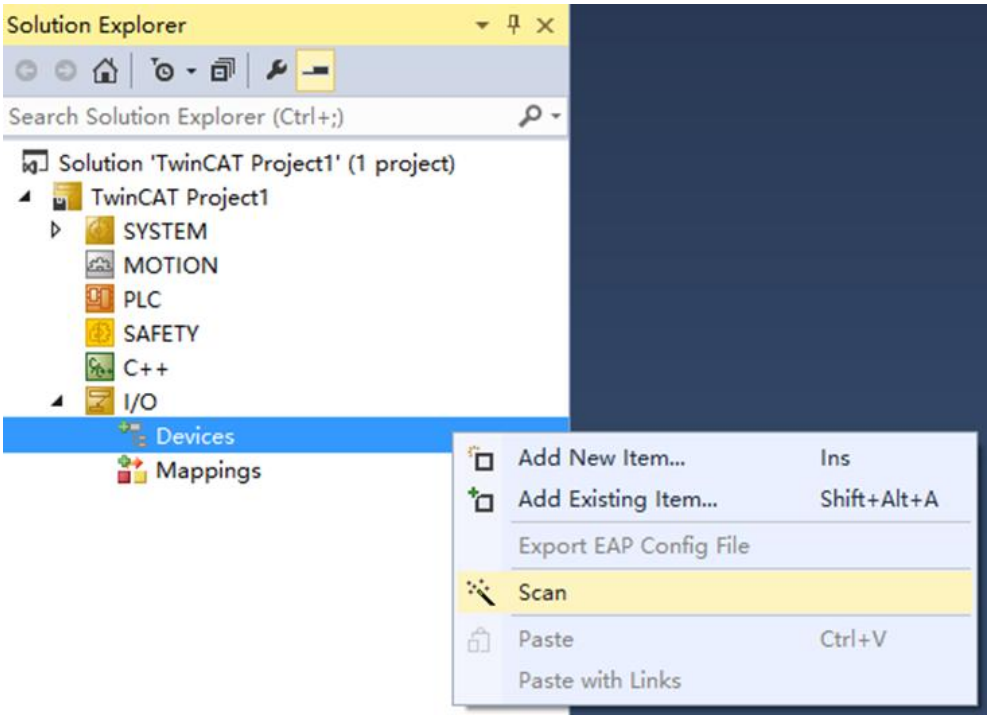
a. Click the TwinCAT icon in the lower right corner of the desktop and select "TwinCAT XAE (VS xxxx)" to open the TwinCAT software, as shown in the figure below.

b. Click "New TwinCAT Project". In the pop-up window, "Name" and "Solution name" correspond to the project name and solution name respectively, and "Location" corresponds to the project path. You can select the default for these three items, then click "OK". The project is created successfully, as shown in the figure below.

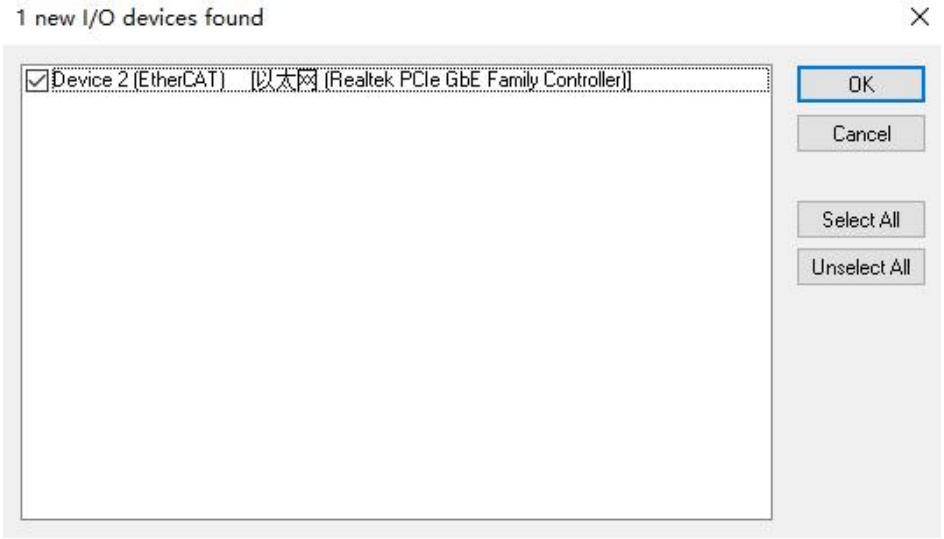


4、Scan Devices

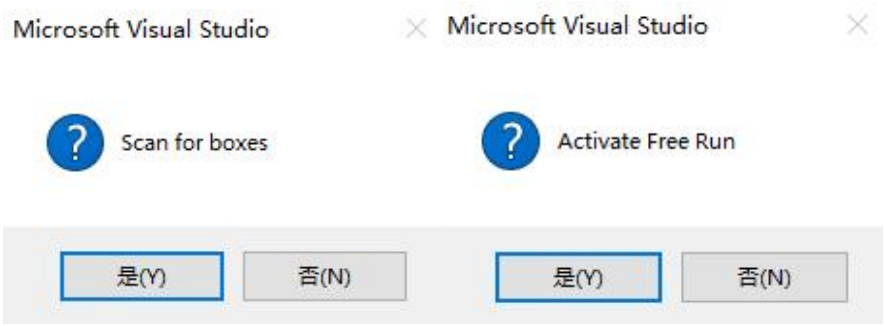
a. After creating the project, right-click the "Scan" option under "I/O -> Devices" to scan the slave devices, as shown in the figure below.



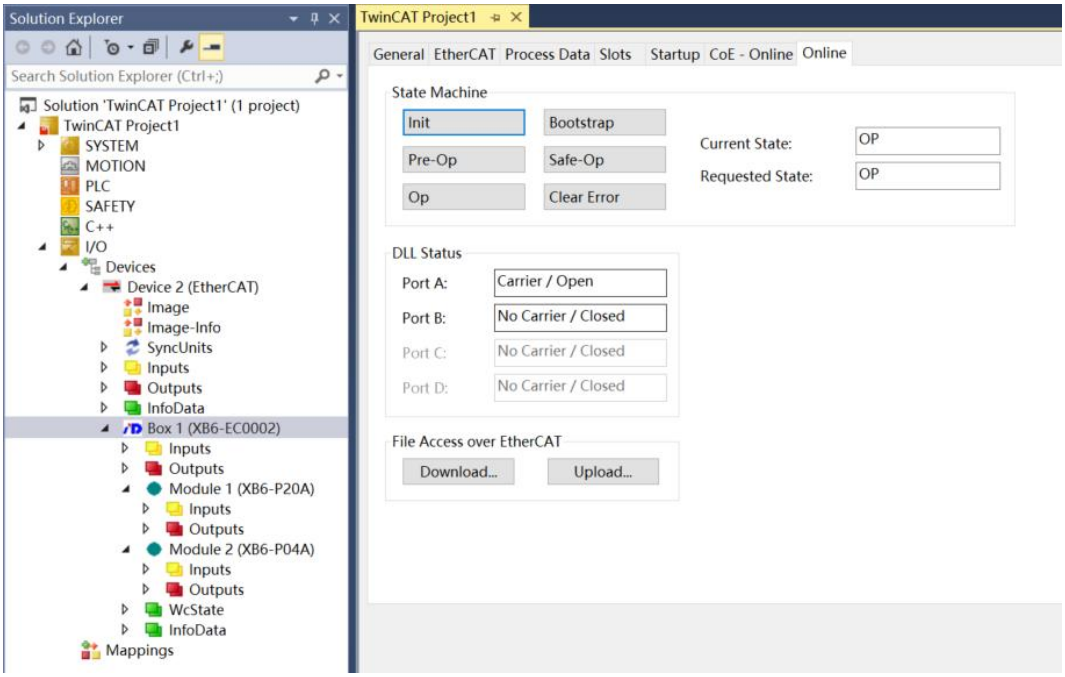
b. Check the "Local Area Connection" network card, as shown in the figure below.



c. In the pop-up window "Scan for boxes", click and select "Yes"; in the pop-up window "Activate Free Run", click and select "Yes", as shown in the following figure.

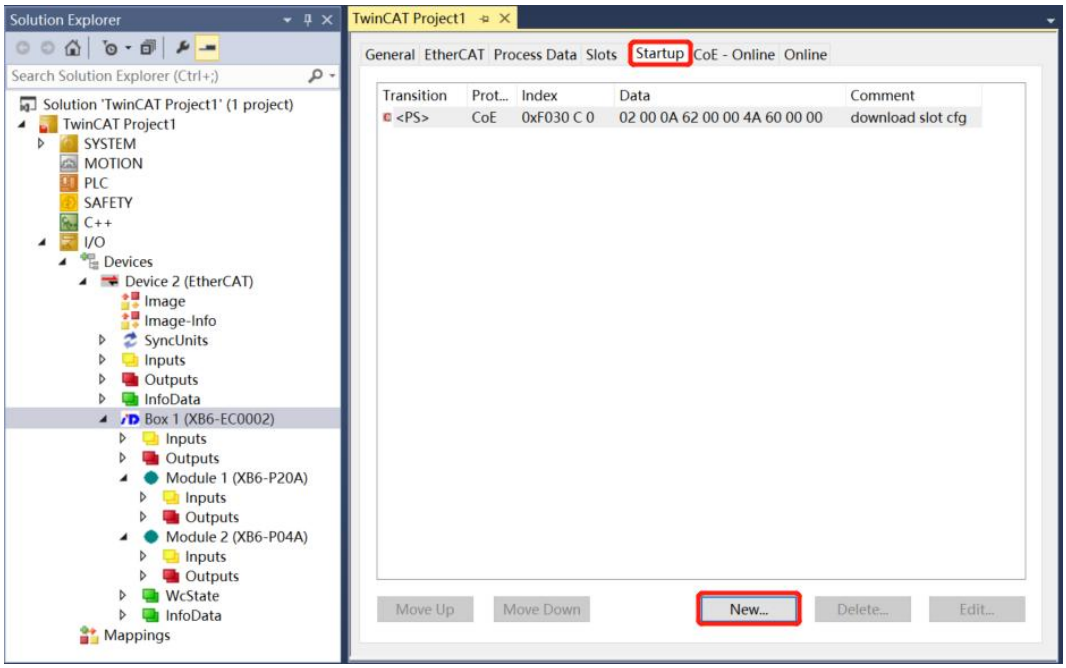


d. After scanning the device, you can see Box1 (XB6-EC0002) and Module 1 (XB6-P20A) in the left navigation tree. In "Online", you can see that TwinCAT is in "OP" state, and the RUN light of the slave device is always on, as shown in the following figure.

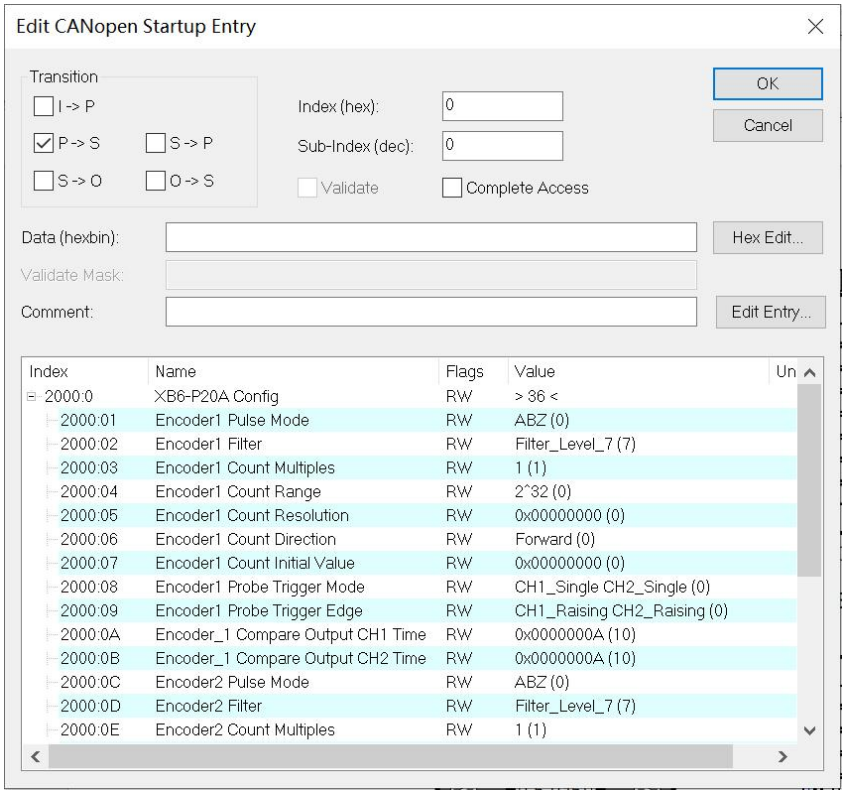


5、Verify basic functionality

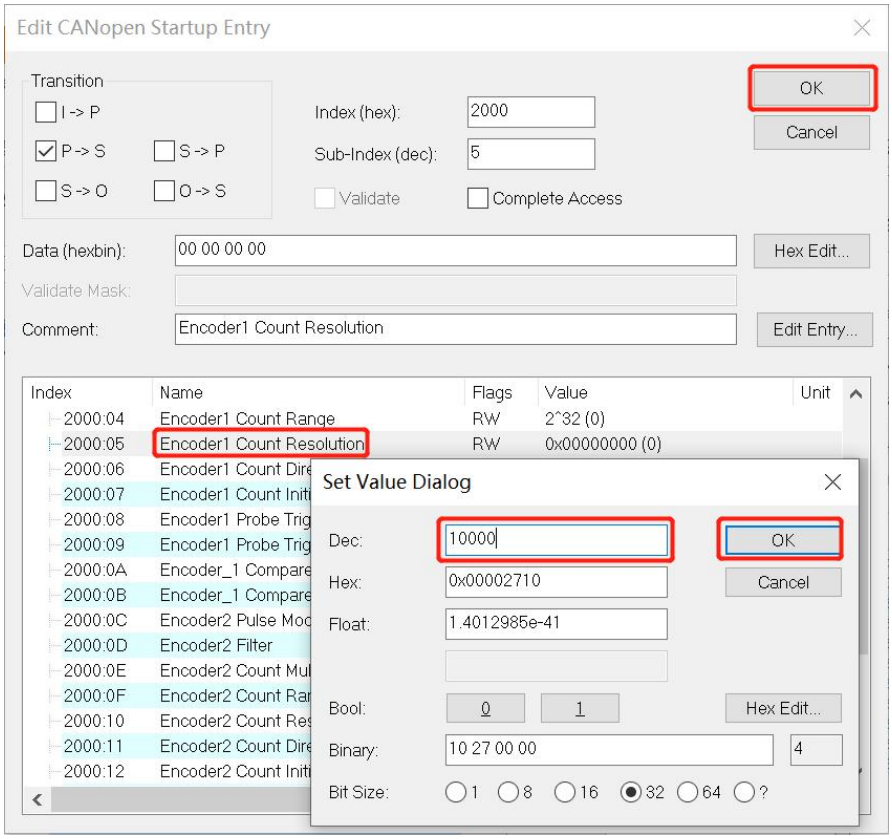
a. Click "Box1 -> Startup -> New" in the left navigation tree to enter the configuration parameter editing page, as shown in the figure below.



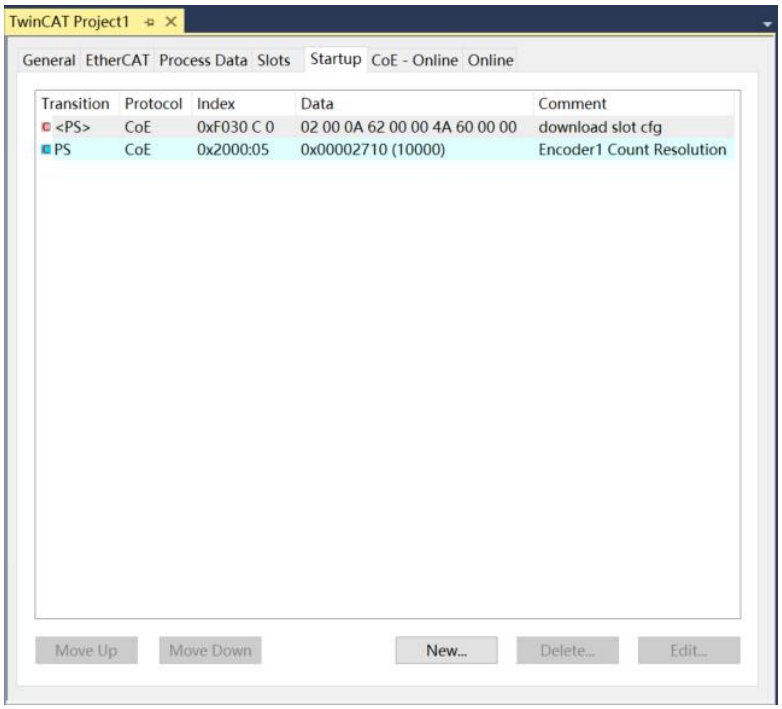
b. In the Edit CANopen Startup Entry pop-up window, click the "+" in front of Index 2000:0 to expand the configuration parameter menu. You can see 24 configuration parameters. Click any parameter to set the related configuration, as shown in the figure below.



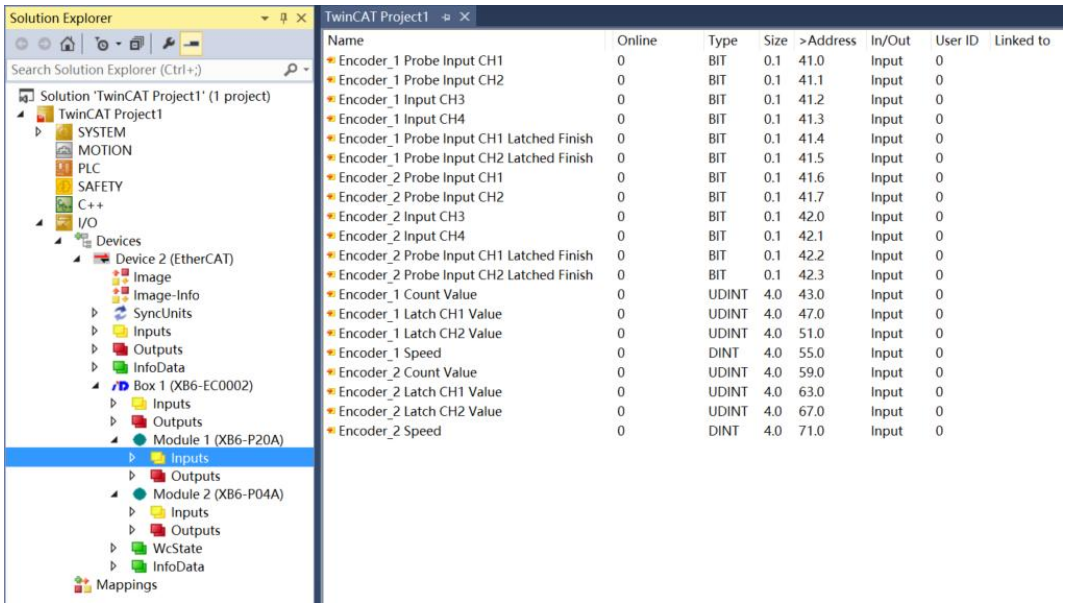
c. For example, to modify the encoder 1 ring count resolution parameter, double-click "Encoder1 Count Resolution" and modify the parameter value, as shown in the figure below.



d. After the parameter modification is completed, the modified parameter items and parameter values can be seen under Startup, as shown in the figure below. After the parameter setting is completed, the Reload operation and the module power-on are required to realize the automatic transmission of parameter settings by the master station.

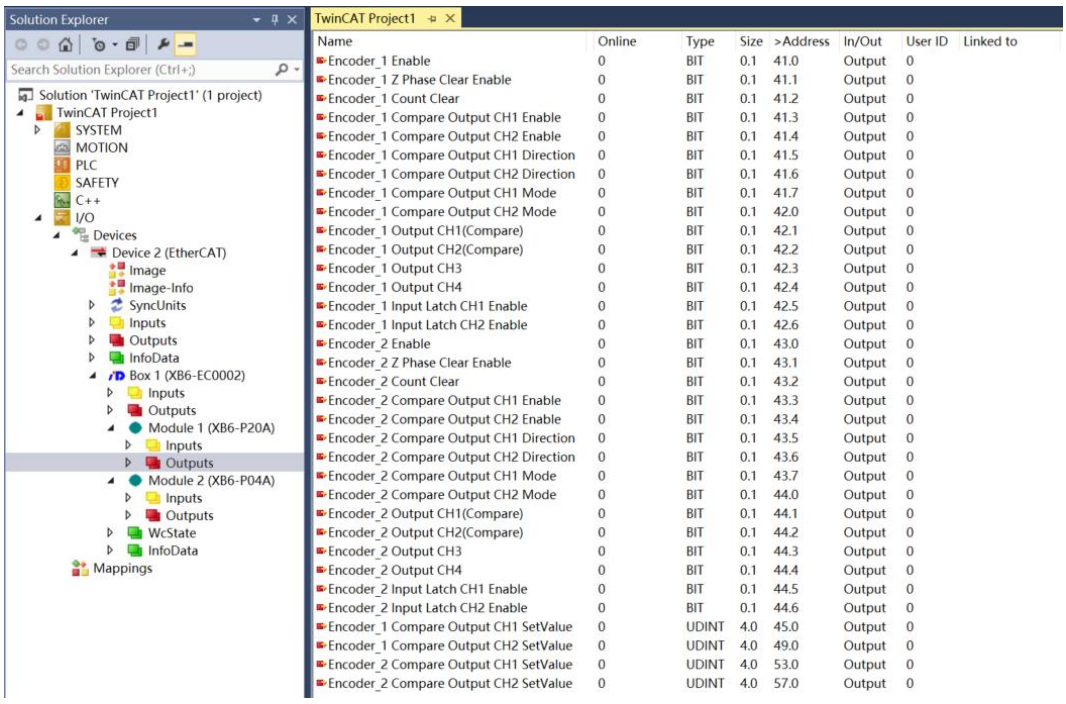


e. The left navigation tree "Module 1 -> Inputs" displays the upstream data of the module and is used to monitor the input of the module, as shown in the following figure.



Name	Online	Type	Size	>Address	In/Out	User ID	Linked to
Encoder_1 Probe Input CH1	0	BIT	0.1	41.0	Input	0	
Encoder_1 Probe Input CH2	0	BIT	0.1	41.1	Input	0	
Encoder_1 Input CH3	0	BIT	0.1	41.2	Input	0	
Encoder_1 Input CH4	0	BIT	0.1	41.3	Input	0	
Encoder_1 Probe Input CH1 Latched Finish	0	BIT	0.1	41.4	Input	0	
Encoder_1 Probe Input CH2 Latched Finish	0	BIT	0.1	41.5	Input	0	
Encoder_2 Probe Input CH1	0	BIT	0.1	41.6	Input	0	
Encoder_2 Probe Input CH2	0	BIT	0.1	41.7	Input	0	
Encoder_2 Input CH3	0	BIT	0.1	42.0	Input	0	
Encoder_2 Input CH4	0	BIT	0.1	42.1	Input	0	
Encoder_2 Probe Input CH1 Latched Finish	0	BIT	0.1	42.2	Input	0	
Encoder_2 Probe Input CH2 Latched Finish	0	BIT	0.1	42.3	Input	0	
Encoder_1 Count Value	0	UDINT	4.0	43.0	Input	0	
Encoder_1 Latch CH1 Value	0	UDINT	4.0	47.0	Input	0	
Encoder_1 Latch CH2 Value	0	UDINT	4.0	51.0	Input	0	
Encoder_1 Speed	0	DINT	4.0	55.0	Input	0	
Encoder_2 Count Value	0	UDINT	4.0	59.0	Input	0	
Encoder_2 Latch CH1 Value	0	UDINT	4.0	63.0	Input	0	
Encoder_2 Latch CH2 Value	0	UDINT	4.0	67.0	Input	0	
Encoder_2 Speed	0	DINT	4.0	71.0	Input	0	

f. The left navigation tree "Module 1 -> Outputs" displays the downstream data of the module, which is used to control the output of the module, as shown in the following figure.



Name	Online	Type	Size	>Address	In/Out	User ID	Linked to
Encoder_1 Enable	0	BIT	0.1	41.0	Output	0	
Encoder_1 Z Phase Clear Enable	0	BIT	0.1	41.1	Output	0	
Encoder_1 Count Clear	0	BIT	0.1	41.2	Output	0	
Encoder_1 Compare Output CH1 Enable	0	BIT	0.1	41.3	Output	0	
Encoder_1 Compare Output CH2 Enable	0	BIT	0.1	41.4	Output	0	
Encoder_1 Compare Output CH1 Direction	0	BIT	0.1	41.5	Output	0	
Encoder_1 Compare Output CH2 Direction	0	BIT	0.1	41.6	Output	0	
Encoder_1 Compare Output CH1 Mode	0	BIT	0.1	41.7	Output	0	
Encoder_1 Compare Output CH2 Mode	0	BIT	0.1	42.0	Output	0	
Encoder_1 Output CH1(Compare)	0	BIT	0.1	42.1	Output	0	
Encoder_1 Output CH2(Compare)	0	BIT	0.1	42.2	Output	0	
Encoder_1 Output CH3	0	BIT	0.1	42.3	Output	0	
Encoder_1 Output CH4	0	BIT	0.1	42.4	Output	0	
Encoder_1 Input Latch CH1 Enable	0	BIT	0.1	42.5	Output	0	
Encoder_1 Input Latch CH2 Enable	0	BIT	0.1	42.6	Output	0	
Encoder_2 Enable	0	BIT	0.1	43.0	Output	0	
Encoder_2 Z Phase Clear Enable	0	BIT	0.1	43.1	Output	0	
Encoder_2 Count Clear	0	BIT	0.1	43.2	Output	0	
Encoder_2 Compare Output CH1 Enable	0	BIT	0.1	43.3	Output	0	
Encoder_2 Compare Output CH2 Enable	0	BIT	0.1	43.4	Output	0	
Encoder_2 Compare Output CH1 Direction	0	BIT	0.1	43.5	Output	0	
Encoder_2 Compare Output CH2 Direction	0	BIT	0.1	43.6	Output	0	
Encoder_2 Compare Output CH1 Mode	0	BIT	0.1	43.7	Output	0	
Encoder_2 Compare Output CH2 Mode	0	BIT	0.1	44.0	Output	0	
Encoder_2 Output CH1(Compare)	0	BIT	0.1	44.1	Output	0	
Encoder_2 Output CH2(Compare)	0	BIT	0.1	44.2	Output	0	
Encoder_2 Output CH3	0	BIT	0.1	44.3	Output	0	
Encoder_2 Output CH4	0	BIT	0.1	44.4	Output	0	
Encoder_2 Input Latch CH1 Enable	0	BIT	0.1	44.5	Output	0	
Encoder_2 Input Latch CH2 Enable	0	BIT	0.1	44.6	Output	0	
Encoder_1 Compare Output CH1 SetValue	0	UDINT	4.0	45.0	Output	0	
Encoder_1 Compare Output CH2 SetValue	0	UDINT	4.0	49.0	Output	0	
Encoder_2 Compare Output CH1 SetValue	0	UDINT	4.0	53.0	Output	0	
Encoder_2 Compare Output CH2 SetValue	0	UDINT	4.0	57.0	Output	0	

Module Functionality Examples

- **Encoder 1 inputs AB quadrature pulses, the number of pulses is 40,000, and encoder 1 probe input channel 1 is latched**

a. Configure the configuration parameters as shown in the following figure.

a) The encoder 1 pulse mode is set to AB quadrature pulse mode, that is, Encoder1 Pulse Mode is set to 0: ABZ;

b) The encoder 1 count multiple is set to 4 times, that is, Encoder1 Count Multiples is set to 4;

c) The encoder 1 count range is set to 0~ring count resolution×count multiples-1, that is, Encoder1 Count Range is set to 1: Resolution×Multiples;

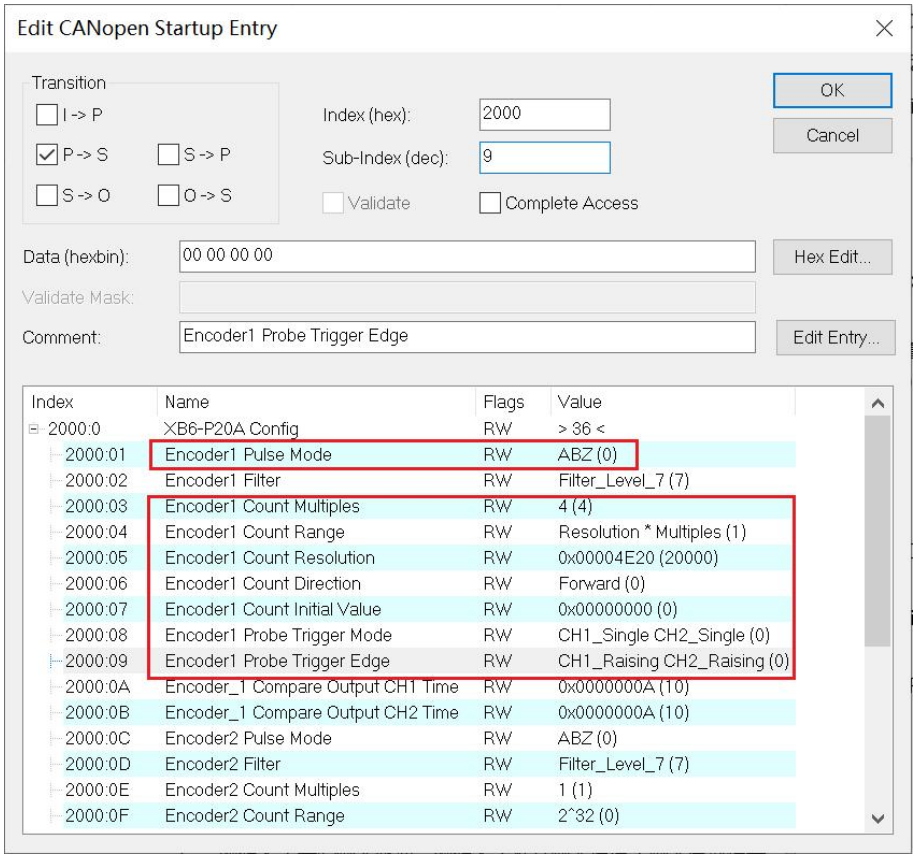
d) The encoder 1 ring count resolution is set to 20000, that is, Encoder1 Count Resolution is set to 20000;

e) The encoder 1 counting direction is set to forward counting, that is, Encoder1 Count Direction is set to 0: Forward;

f) The initial value of encoder 1 count is set to 0, that is, Encoder1 Count Initial Value is set to 0;

g) The probe mode of encoder 1 is set to single for channel 1 and single for channel 2, that is, Encoder1 Probe Trigger Mode is set to 0: CH1_Single CH2_Single;

h) The encoder 1 probe trigger edge is set to the rising edge of channel 1 and the rising edge of channel 2, that is, Encoder1 Probe Trigger Edge is set to 0: CH1_Raising CH2_Raising.

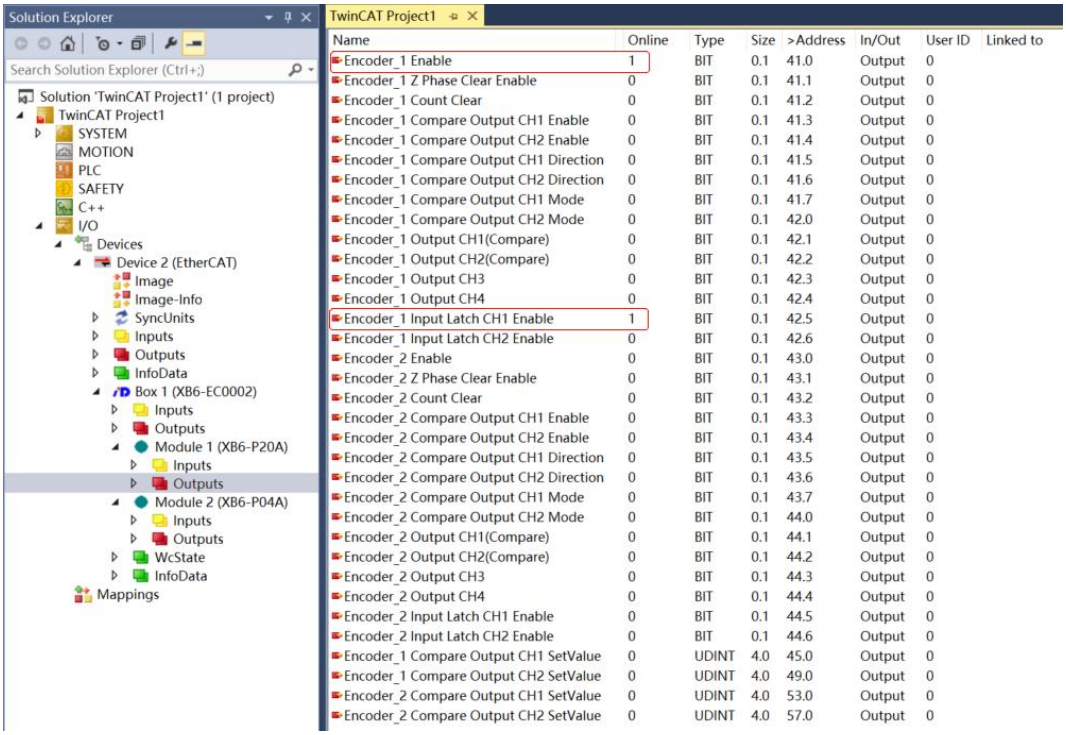


After the parameter setting is completed, the Reload operation is required and the module is powered on again to enable the master station to automatically send the parameter settings.

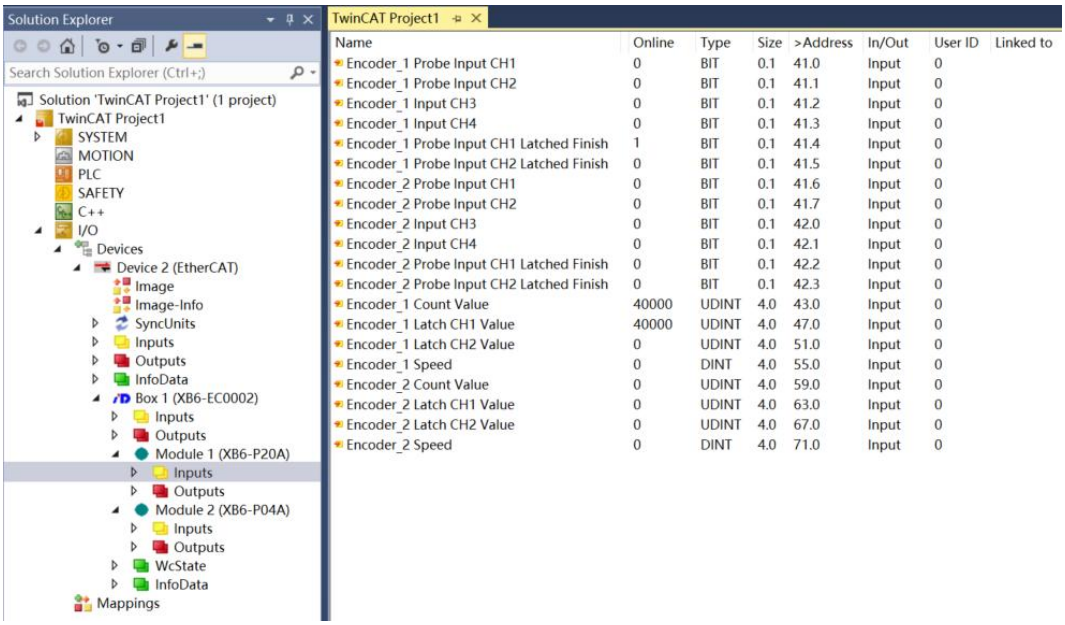
b. Set encoder 1 count enable and encoder 1 probe input channel 1 latch enable, as shown in the figure below.

a) Downlink data Encoder_1 Enable is set to 1;

b) Set the downstream data Encoder_1 Input Latch CH1 Enable to 1.



c. Encoder 1 starts to input 40,000 pulses. After the pulse counting is completed, encoder 1 probe input channel 1 inputs a valid signal, the encoder 1 count value is 40,000, the probe input channel 1 latch value is 40,000, and the encoder probe input channel 1 latch completion flag value flips once to 1, as shown in the figure below.



- **Encoder 1 input direction pulse, pulse quantity 40000, encoder 1 comparison output channel 1 comparison output**

a. Configure the configuration parameters as shown in the following figure.

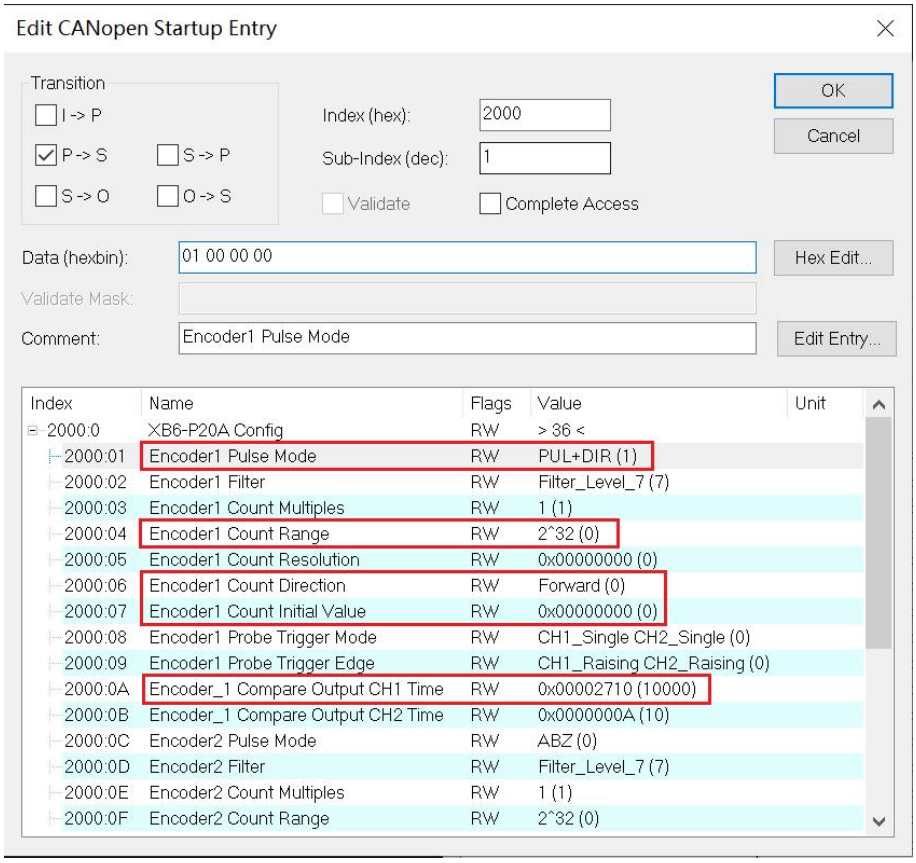
a) The encoder 1 pulse mode is set to the direction pulse mode, that is, Encoder1 Pulse Mode is set to 1: Pul+Dir;

b) The encoder 1 count range is set to 0~2^32-1, that is, Encoder1 Count Range is set to 0:2^32;

c) The encoder 1 counting direction is set to forward counting, that is, Encoder1 Count Direction is set to 0: Forward;

d) The initial value of encoder 1 count is set to 0, that is, Encoder1 Count Initial Value is set to 0;

e) The encoder 1 compare output channel 1 pulse time is set to 10s, that is, Encoder1 Compare Output CH1 Time is set to 10000.



After the parameter setting is completed, the Reload operation is required and the module is powered on again to enable the master station to automatically send the parameter settings.

b. Set encoder 1 counting enable, encoder 1 comparison output channel 1 set comparison set value, comparison direction and comparison mode and enable, as shown in the following figure.

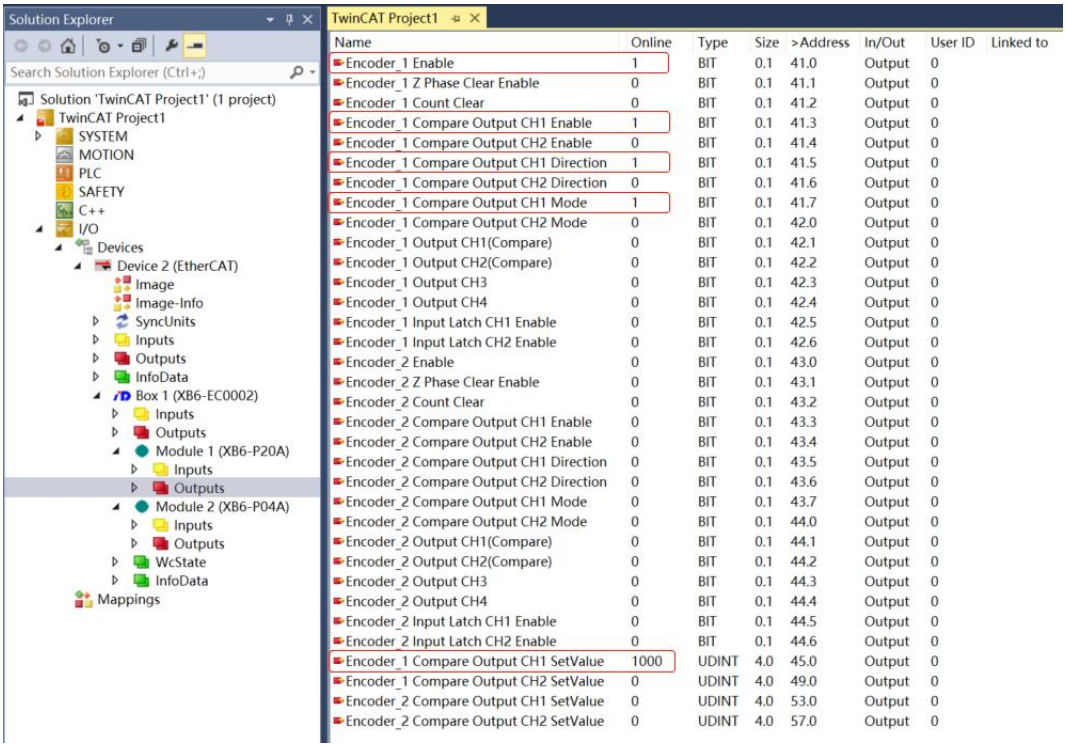
a) Downlink data Encoder_1 Enable is set to 1;

b) Downlink data Encoder_1 Compare Output CH1 SetValue is set to 1000;

c) Downlink data Encoder_1 Compare Output CH1 Direction is set to 1 for incremental comparison;

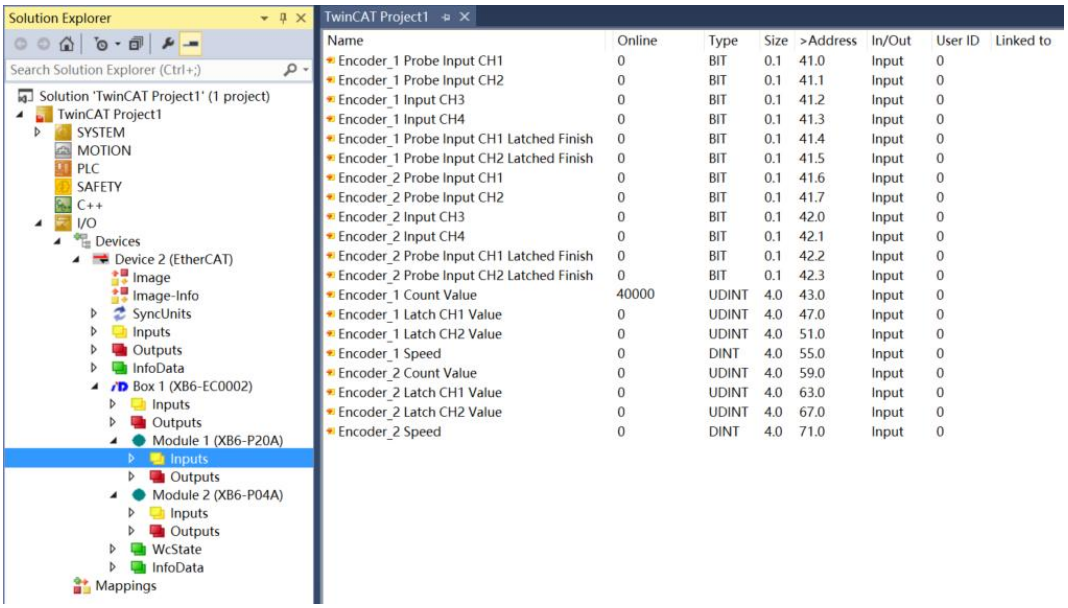
d) Downlink data Encoder_1 Compare Output CH1 Mode is set to 1 Repeat Trigger;

e) Set the downstream data Encoder_1 Compare Output CH1 Enable to 1 to enable.



Name	Online	Type	Size	>Address	In/Out	User ID	Linked to
Encoder_1 Enable	1	BIT	0.1	41.0	Output	0	
Encoder_1 Z Phase Clear Enable	0	BIT	0.1	41.1	Output	0	
Encoder_1 Count Clear	0	BIT	0.1	41.2	Output	0	
Encoder_1 Compare Output CH1 Enable	1	BIT	0.1	41.3	Output	0	
Encoder_1 Compare Output CH2 Enable	0	BIT	0.1	41.4	Output	0	
Encoder_1 Compare Output CH1 Direction	1	BIT	0.1	41.5	Output	0	
Encoder_1 Compare Output CH2 Direction	0	BIT	0.1	41.6	Output	0	
Encoder_1 Compare Output CH1 Mode	1	BIT	0.1	41.7	Output	0	
Encoder_1 Compare Output CH2 Mode	0	BIT	0.1	42.0	Output	0	
Encoder_1 Output CH1(Compare)	0	BIT	0.1	42.1	Output	0	
Encoder_1 Output CH2(Compare)	0	BIT	0.1	42.2	Output	0	
Encoder_1 Output CH3	0	BIT	0.1	42.3	Output	0	
Encoder_1 Output CH4	0	BIT	0.1	42.4	Output	0	
Encoder_1 Input Latch CH1 Enable	0	BIT	0.1	42.5	Output	0	
Encoder_1 Input Latch CH2 Enable	0	BIT	0.1	42.6	Output	0	
Encoder_2 Enable	0	BIT	0.1	43.0	Output	0	
Encoder_2 Z Phase Clear Enable	0	BIT	0.1	43.1	Output	0	
Encoder_2 Count Clear	0	BIT	0.1	43.2	Output	0	
Encoder_2 Compare Output CH1 Enable	0	BIT	0.1	43.3	Output	0	
Encoder_2 Compare Output CH2 Enable	0	BIT	0.1	43.4	Output	0	
Encoder_2 Compare Output CH1 Direction	0	BIT	0.1	43.5	Output	0	
Encoder_2 Compare Output CH2 Direction	0	BIT	0.1	43.6	Output	0	
Encoder_2 Compare Output CH1 Mode	0	BIT	0.1	43.7	Output	0	
Encoder_2 Compare Output CH2 Mode	0	BIT	0.1	44.0	Output	0	
Encoder_2 Output CH1(Compare)	0	BIT	0.1	44.1	Output	0	
Encoder_2 Output CH2(Compare)	0	BIT	0.1	44.2	Output	0	
Encoder_2 Output CH3	0	BIT	0.1	44.3	Output	0	
Encoder_2 Output CH4	0	BIT	0.1	44.4	Output	0	
Encoder_2 Input Latch CH1 Enable	0	BIT	0.1	44.5	Output	0	
Encoder_2 Input Latch CH2 Enable	0	BIT	0.1	44.6	Output	0	
Encoder_1 Compare Output CH1 SetValue	1000	UDINT	4.0	45.0	Output	0	
Encoder_1 Compare Output CH2 SetValue	0	UDINT	4.0	49.0	Output	0	
Encoder_2 Compare Output CH1 SetValue	0	UDINT	4.0	53.0	Output	0	
Encoder_2 Compare Output CH2 SetValue	0	UDINT	4.0	57.0	Output	0	

c. Encoder 1 starts to input 40,000 pulses. The count value goes up from 0. When it reaches 1,000 (satisfying the comparison setting value and direction), the comparison output channel 1 state flips from the original low-level output to high-level output. The pulse output time is 10s, and the channel indicator light will be on for 10s. After the counting is completed, the encoder 1 count value is 40,000, as shown in the figure below.



Name	Online	Type	Size	>Address	In/Out	User ID	Linked to
Encoder_1 Probe Input CH1	0	BIT	0.1	41.0	Input	0	
Encoder_1 Probe Input CH2	0	BIT	0.1	41.1	Input	0	
Encoder_1 Input CH3	0	BIT	0.1	41.2	Input	0	
Encoder_1 Input CH4	0	BIT	0.1	41.3	Input	0	
Encoder_1 Probe Input CH1 Latched Finish	0	BIT	0.1	41.4	Input	0	
Encoder_1 Probe Input CH2 Latched Finish	0	BIT	0.1	41.5	Input	0	
Encoder_2 Probe Input CH1	0	BIT	0.1	41.6	Input	0	
Encoder_2 Probe Input CH2	0	BIT	0.1	41.7	Input	0	
Encoder_2 Input CH3	0	BIT	0.1	42.0	Input	0	
Encoder_2 Input CH4	0	BIT	0.1	42.1	Input	0	
Encoder_2 Probe Input CH1 Latched Finish	0	BIT	0.1	42.2	Input	0	
Encoder_2 Probe Input CH2 Latched Finish	0	BIT	0.1	42.3	Input	0	
Encoder_1 Count Value	40000	UDINT	4.0	43.0	Input	0	
Encoder_1 Latch CH1 Value	0	UDINT	4.0	47.0	Input	0	
Encoder_1 Latch CH2 Value	0	UDINT	4.0	51.0	Input	0	
Encoder_1 Speed	0	DINT	4.0	55.0	Input	0	
Encoder_2 Count Value	0	UDINT	4.0	59.0	Input	0	
Encoder_2 Latch CH1 Value	0	UDINT	4.0	63.0	Input	0	
Encoder_2 Latch CH2 Value	0	UDINT	4.0	67.0	Input	0	
Encoder_2 Speed	0	DINT	4.0	71.0	Input	0	

6.4.2 Application in TIA Portal V17 software environment

1、Preparation

- **Hardware Environment**
  - **Module model XB6-P20A**
  - **Power module, PROFINET coupler, end cover**

  This description takes XB6-P2000H power supply and XB6-PN0002 coupler as an example
  - **A computer with TIA Portal V17 software pre-installed**
  - **PROFINET special shielded cable**
  - **Pulse output type sensor and other equipment, this description takes the connection of XB6-P04A module as an example**
  - **A Siemens PLC. This description takes Siemens S7-1200 CPU1214C DC/DC/DC as an example.**
  - **Encoder and other equipment**
  - **Switching power supply**
  - **Module mounting rails and rail fixings**
  - **Device Profile**

    Configuration file acquisition address:https://www.solidotech.com/documents/configfile
- **Hardware configuration and wiring**

  Please follow"4 Installation and removal""5 WiringRequest action

2、New Construction

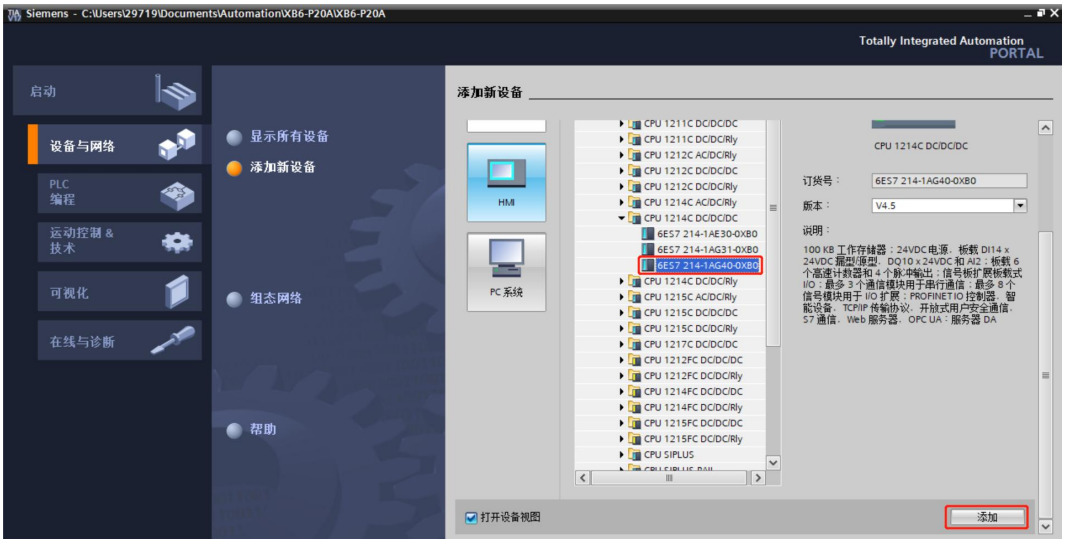
a. Open the TIA Portal V17 software and click "Create New Project".

- Project name: Custom, you can keep the default.
- Path: The project path can be kept as default.
- Version: You can keep the default value.
- Author: You can keep the default value.
- Note: Customized, optional.

3、Add a PLC controller

a. Click "Configure Device", as shown in the following figure.

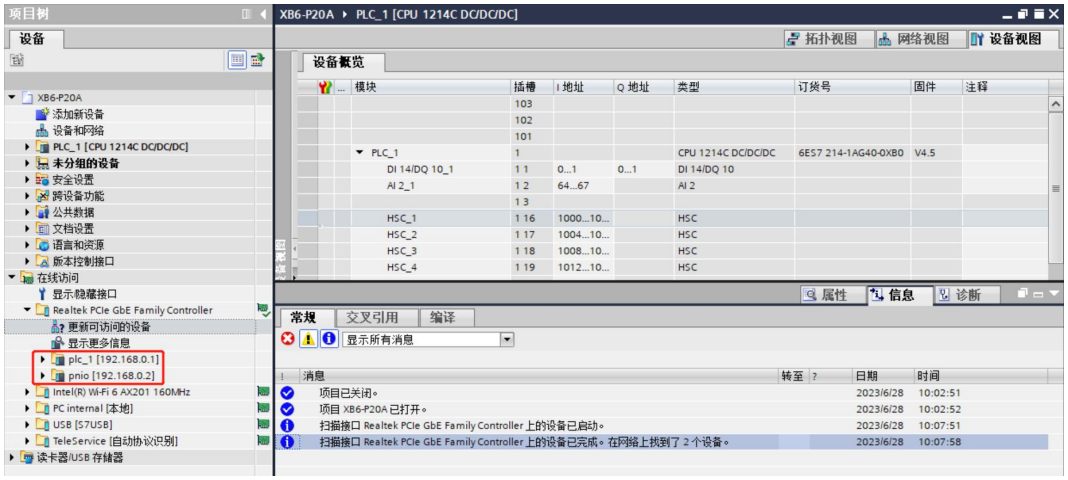
b. Click "Add New Device", select the PLC model currently used, and click "Add", as shown in the figure below. After adding, you can see that the PLC has been added to the device navigation tree.



4、Scan for connected devices

a. Click Online Access -> Update Accessible Devices in the left navigation tree, as shown in the following figure.

b. After the update is completed, the connected slave devices are displayed, as shown in the figure below.



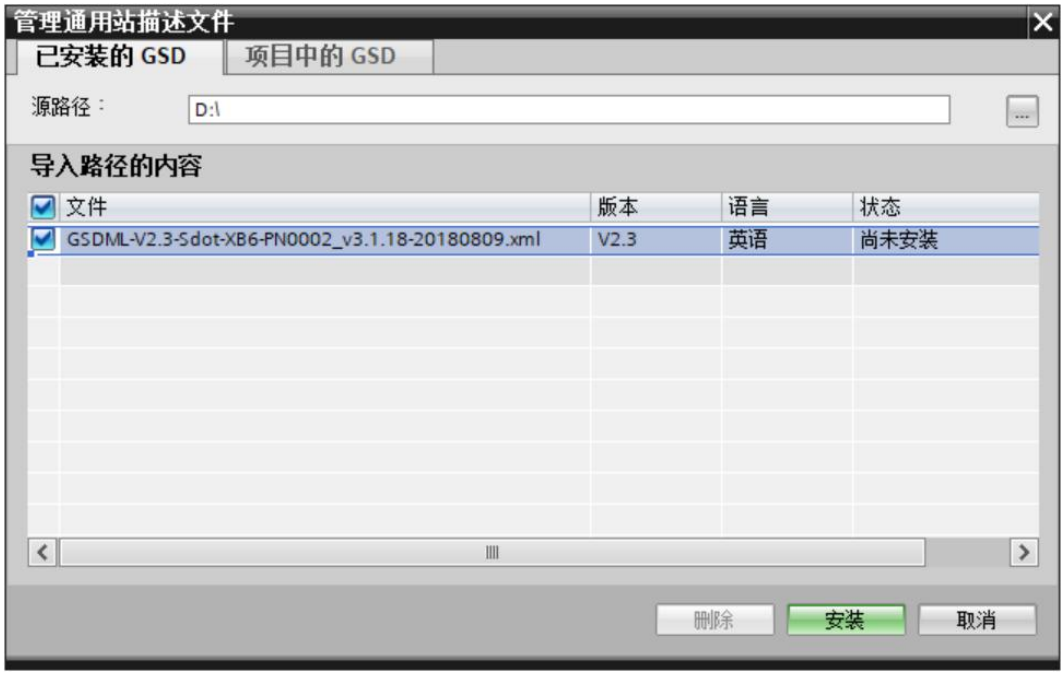
The computer's IP address must be in the same network segment as the PLC. If not, change the computer's IP address and repeat the above steps.

5、Adding a GSD Configuration File

a. In the menu bar, select "Options -> Manage General Station Description File (GSDML) (D)".

b. Click Source Path to select the file.

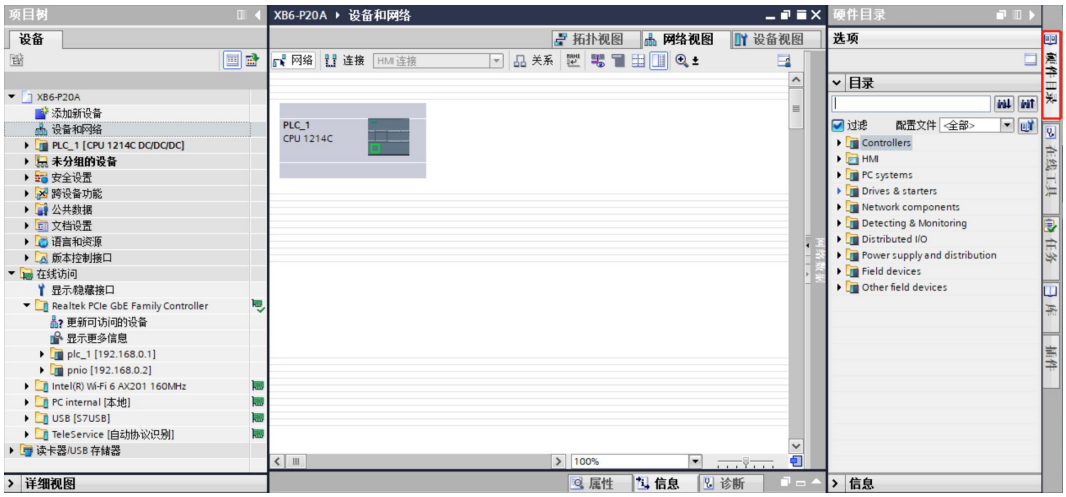
c. Check whether the status of the GSD file to be added is "Not Installed". If it is not installed, click the "Install" button. If it is installed, click "Cancel" to skip the installation step.



6、Adding a slave device

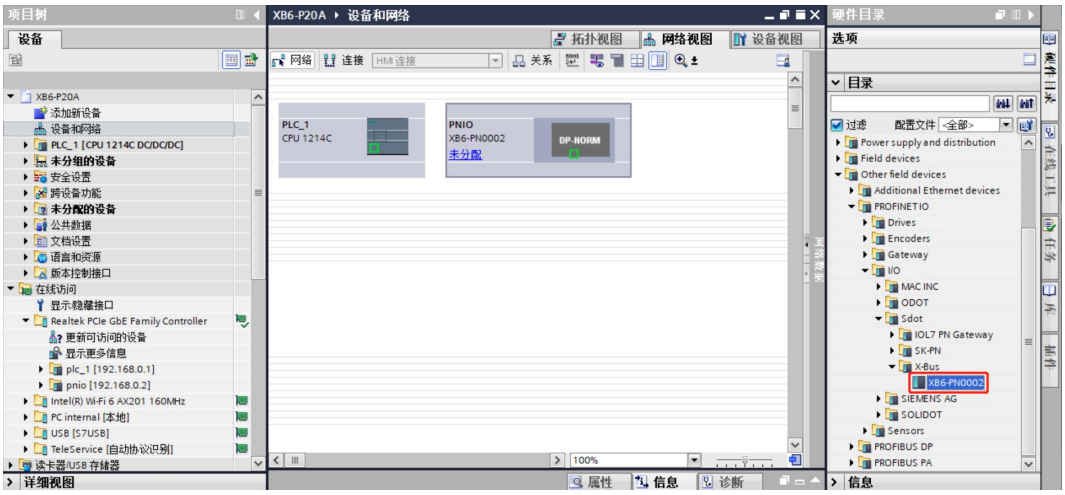
a. Double-click "Devices & Networks" in the left navigation bar.

b. Click the vertical button of "Hardware Catalog" on the right, and the catalog will be displayed as shown in the figure below.

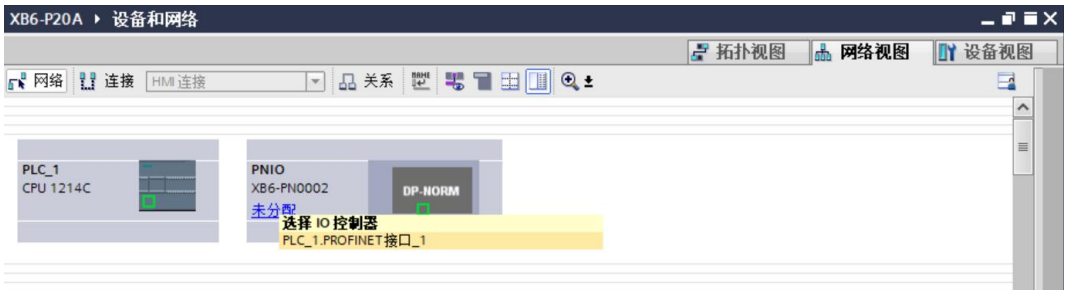


c. Select "Other field devices -> PROFINET IO -> I/O -> Sdot -> X-Bus -> XB6-PN0002".

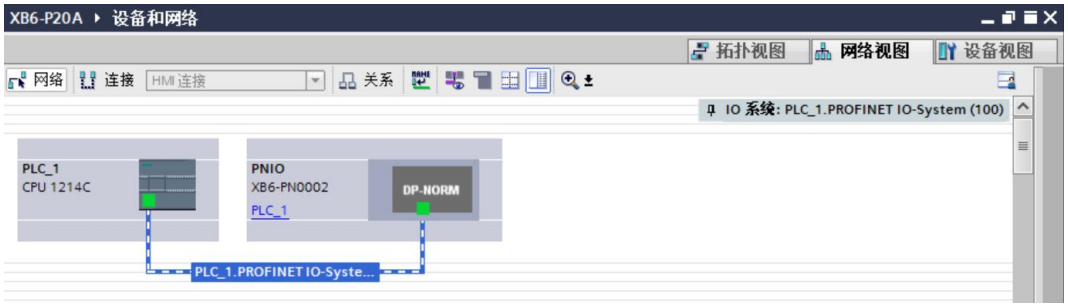
d. Drag or double-click "XB6-PN0002" to the "Network View", as shown in the figure below.



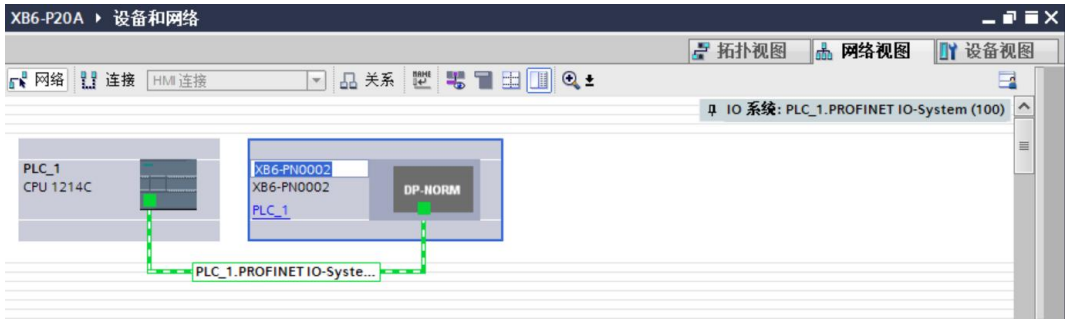
e. Click "Unassigned (blue font)" on the slave device and select "PLC_1.PROFINET Interface_1", as shown in the following figure.



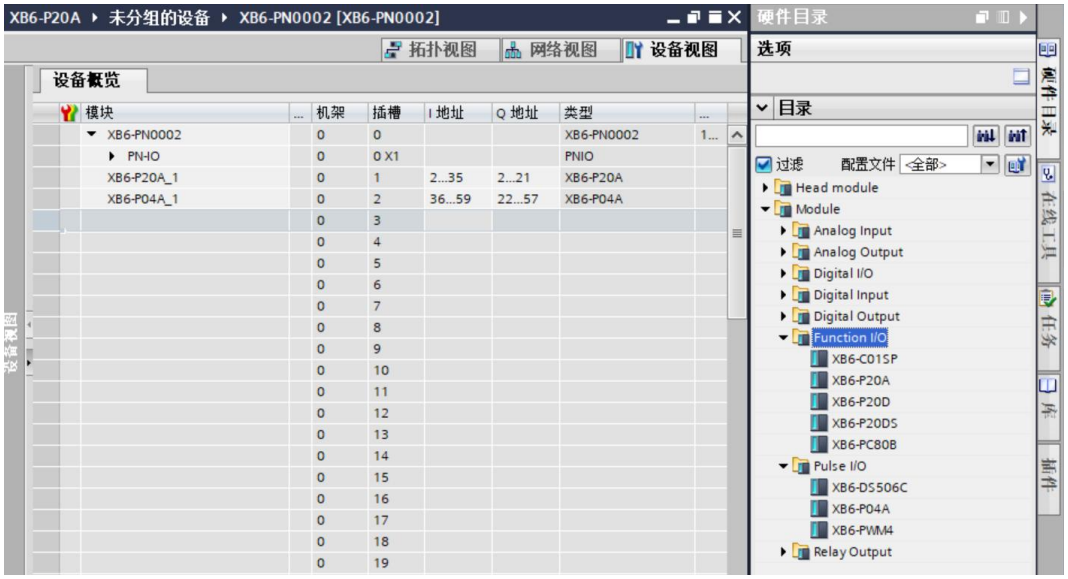
f. After the connection is completed, it will be as shown in the figure below.



g. Click the device name to rename the device, as shown in the following figure.

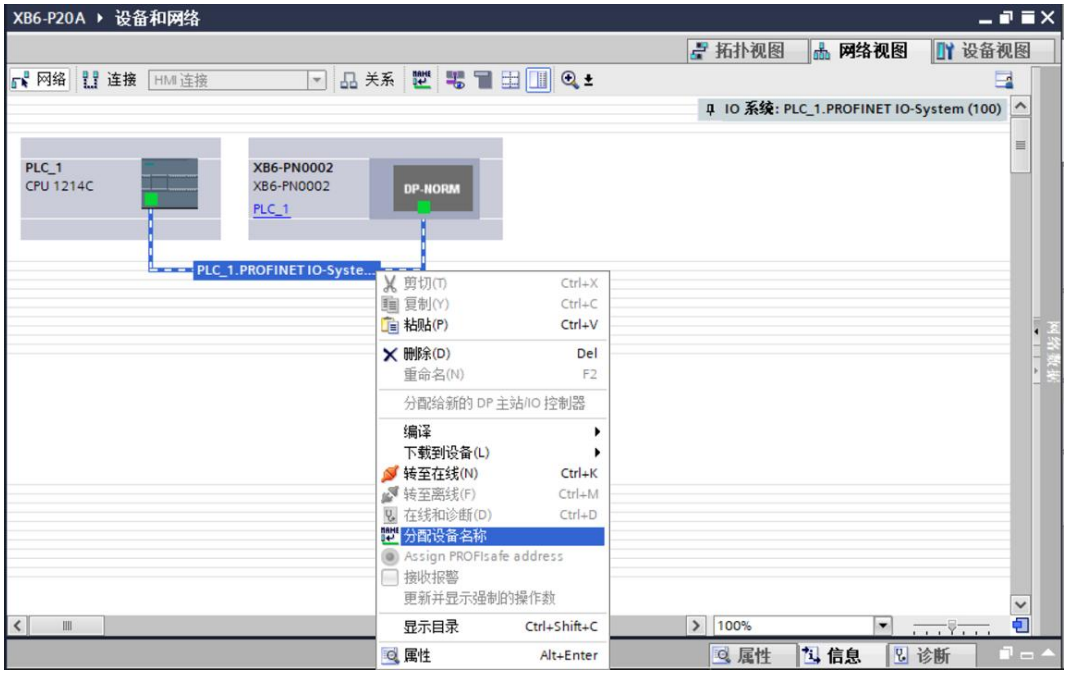


h. Click "Device View" to enter the device overview of the coupler. Under "Hardware Catalog" on the right, add modules in sequence according to the actual topology (the order must be consistent with the actual topology, otherwise communication will not be successful), as shown in the following figure.

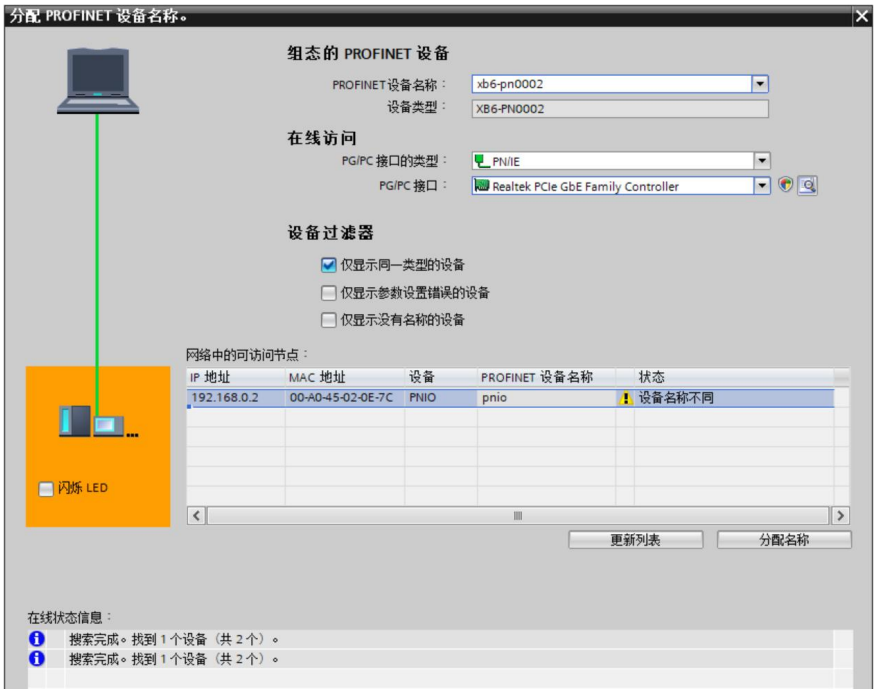


7、Assigning a Device Name

a. Switch to "Network View", right-click the connection line between the PLC and the coupler, and select "Assign Device Name", as shown in the figure below.



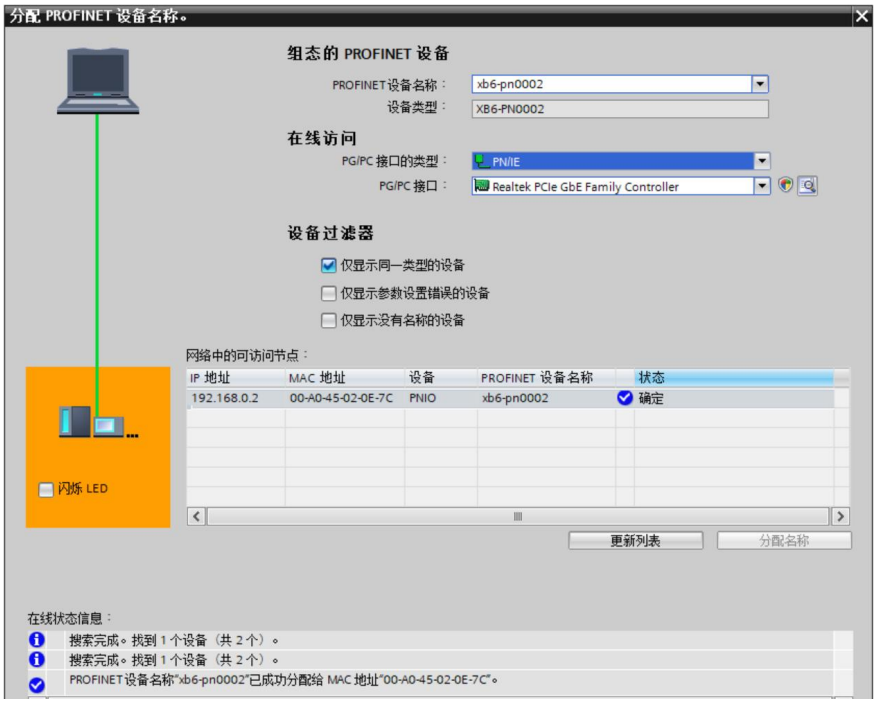
b. The "Assign PROFINET Device Name" window pops up, as shown below.



Check to see if the MAC address printed on the coupler's silkscreen is the same as the MAC address of the assigned device name.

- PROFINET device name: The name set in "Assign IP address and device name to slave".
- Type of PG/PC interface: PN/IE.
- PG/PC interface: The network adapter actually used.

c. Select the slave devices one by one, click Update List, and then click Assign Name. Check whether the node status in Accessible Nodes in Network is OK, as shown in the following figure.



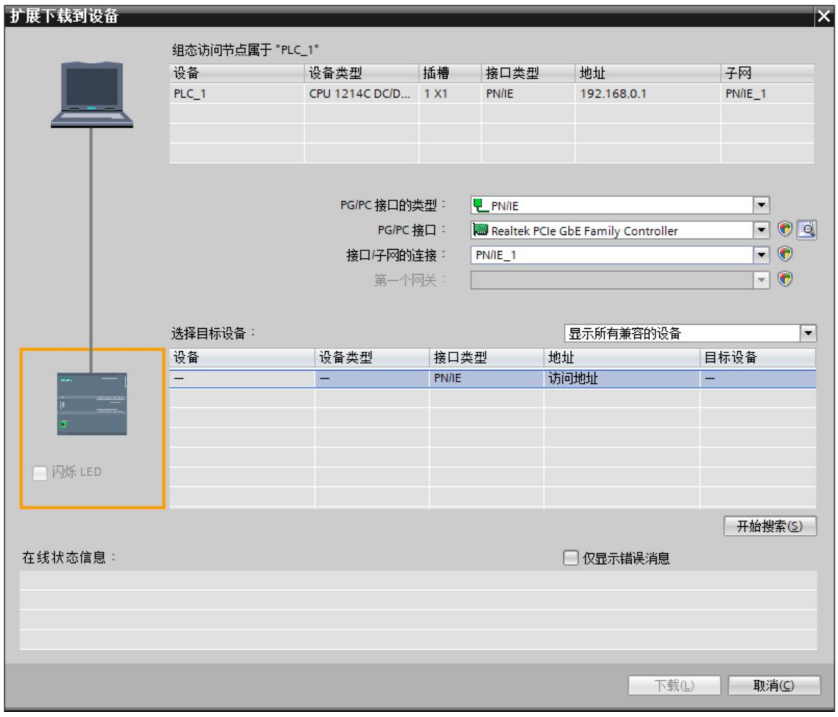
d. Click Close.

8、Downloading the configuration structure

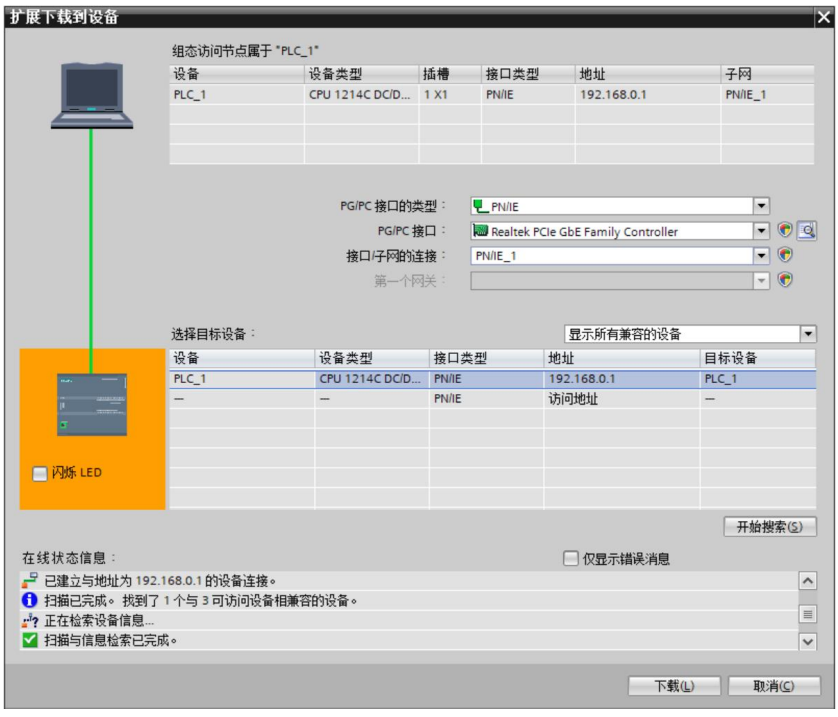
a. In the Network View, select the PLC.

b. Click the button in the menu bar to download the current configuration to the PLC.

c. In the pop-up "Extended Download to Device" interface, configure as shown below.



d. Click Start Search, as shown in the following figure.



e. Click Download.

f. Select "Continue without synchronization", as shown in the following figure.

g. Select Stop All.

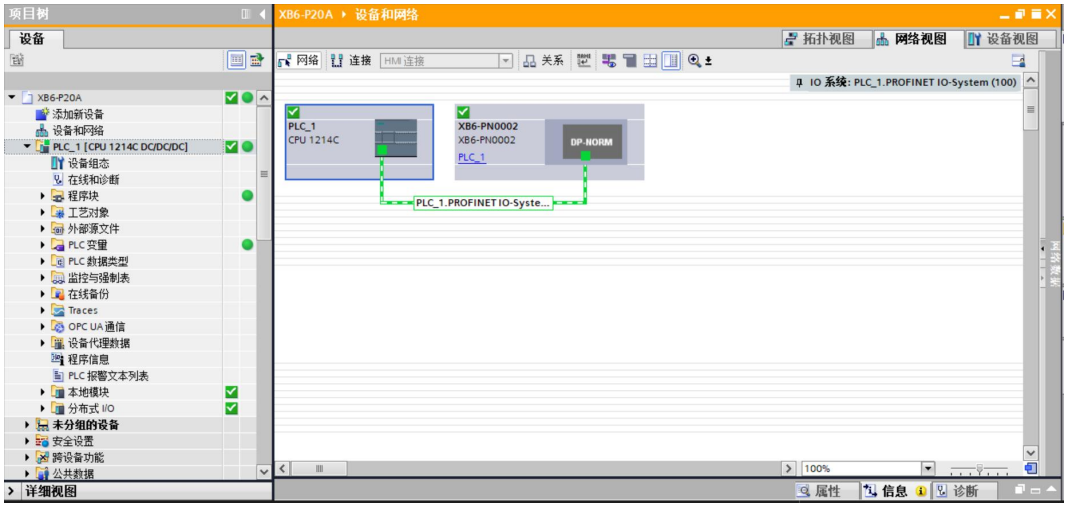
h. Click Mount.

i. Click Finish.

j. Power on the device again.

9、Communication connection

a. Click the button, then click the "Go Online" button. If all icons are green, the connection is successful, as shown in the figure below.



10、 Check the device indicator lights

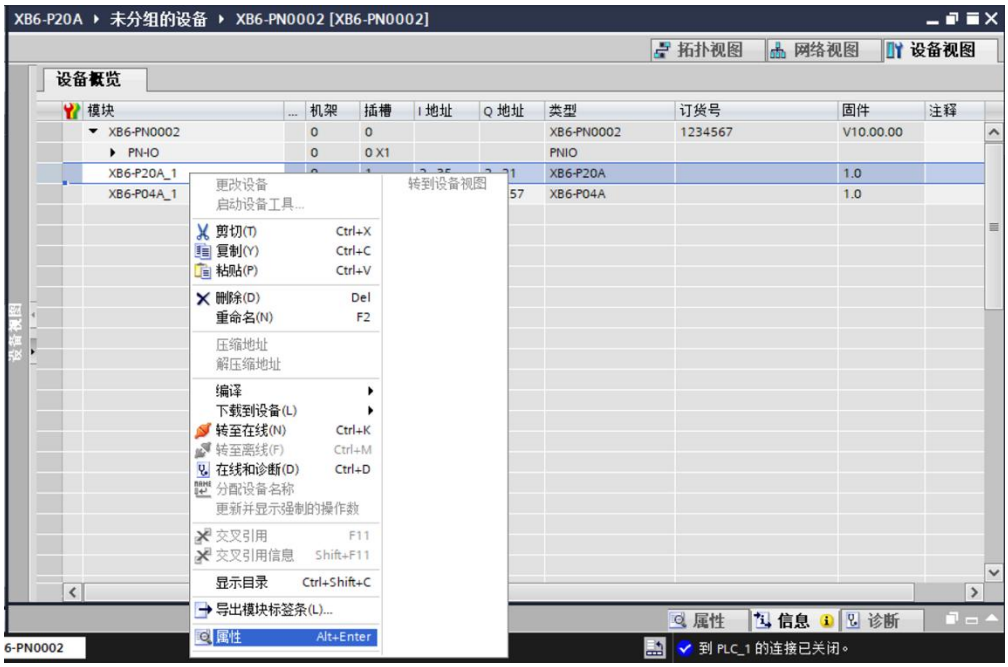
XB6-P2000H: The P light is always green.

XB6-PN0002: The P light is always green, the L light is always on, the B light is off, and the R light is always on.

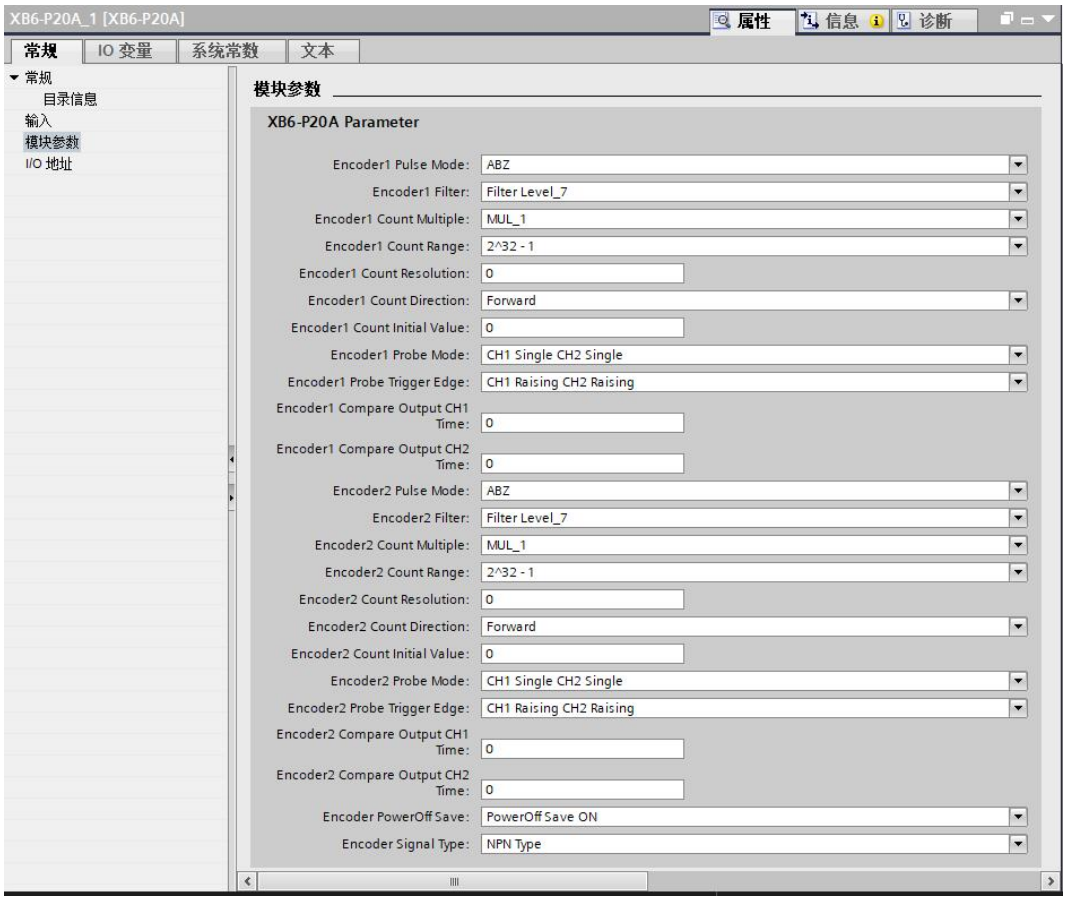
XB6-P20A module: The P light is always on, and the R light is always on.

11、 Parameter settings

a. Open the "Device View", in offline state, right-click the XB6-P20A module, and click "Properties", as shown in the figure below.

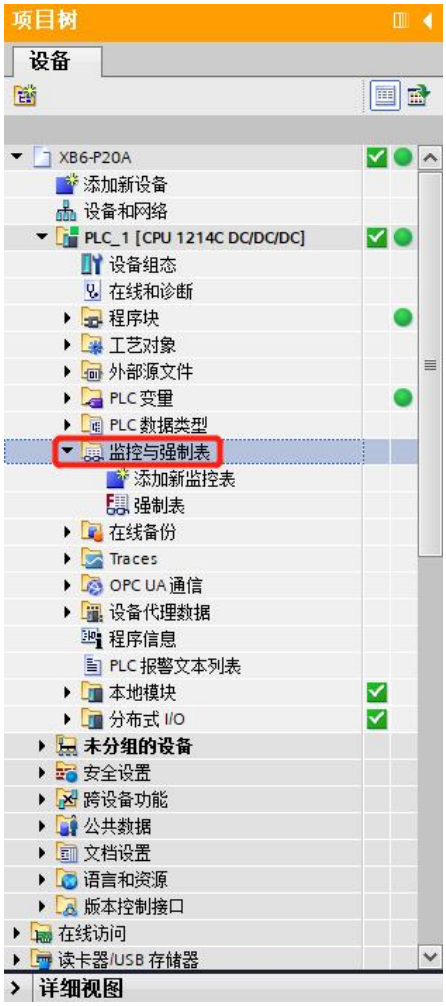


b. On the property page, click "Module Parameters", as shown in the figure below. The parameters can be configured according to actual needs. After the configuration is completed, the program needs to be downloaded to the PLC again, and the PLC and the module need to be powered on again.

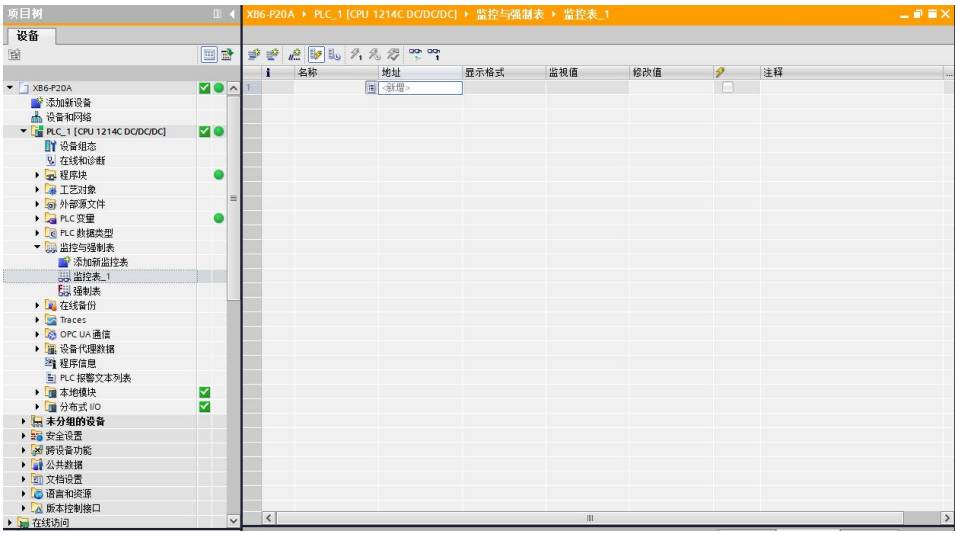


12、 Functional Verification

a. Expand the project navigation on the left and select "Monitoring and Enforcement Tables", as shown in the figure below.



b. Double-click "Add new monitoring table" and the system will add a new monitoring table, as shown in the figure below.



c. Open the "Device View" and check the channel Q address (channel address of the output signal) and I address (channel address of the input signal) of the module XB6-P20A in the device overview.

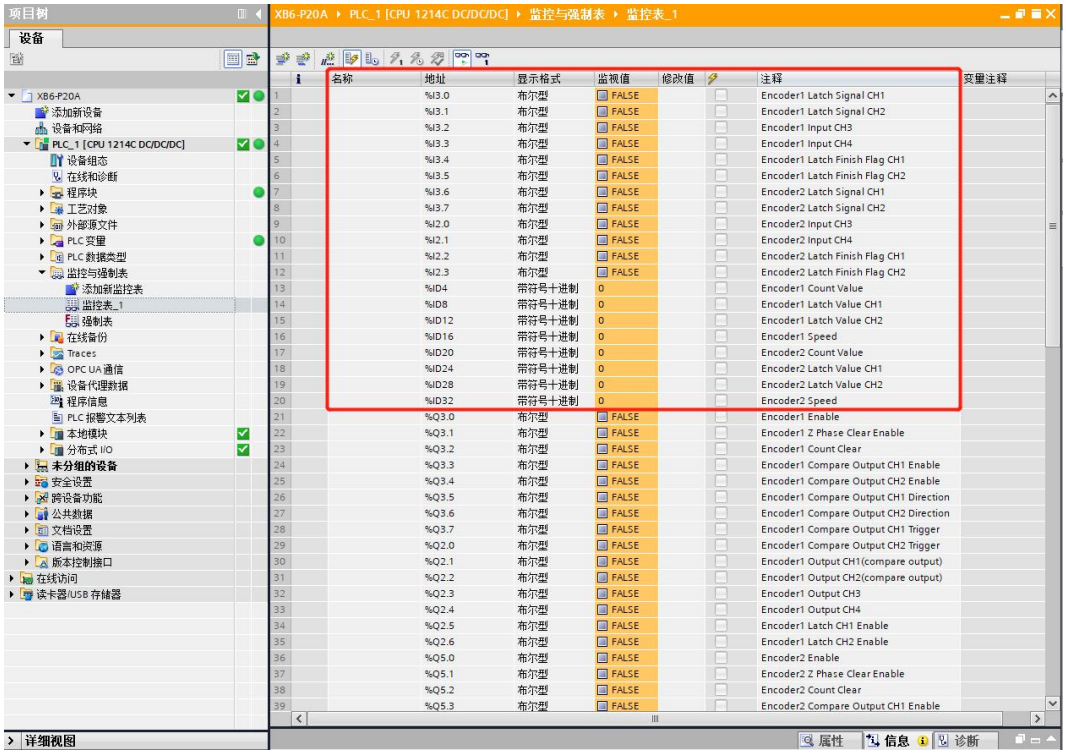
For example, the "I address" of the XB6-P20A module is 2 to 35, and the "Q address" is 2 to 21, as shown in the figure below.

模块	...	机架	插槽	I 地址	Q 地址	类型	订货号	固件	注释
XB6-PN0002		0	0			XB6-PN0002	1234567	V10.00.00	
PN-IO		0	0 X1			PNIO			
XB6-P20A_1		0	1	2...35	2...21	XB6-P20A		1.0	
XB6-P04A_1		0	2	36...59	22...57	XB6-P04A		1.0	
		0	3						
		0	4						

d. Enter the upstream and downstream addresses, data types and comments in the monitoring table address cells for easy monitoring. You can refer to the upstream and downstream process data definitions, enter the data items in sequence, press the "Enter" key, and click  Button, monitor the data.

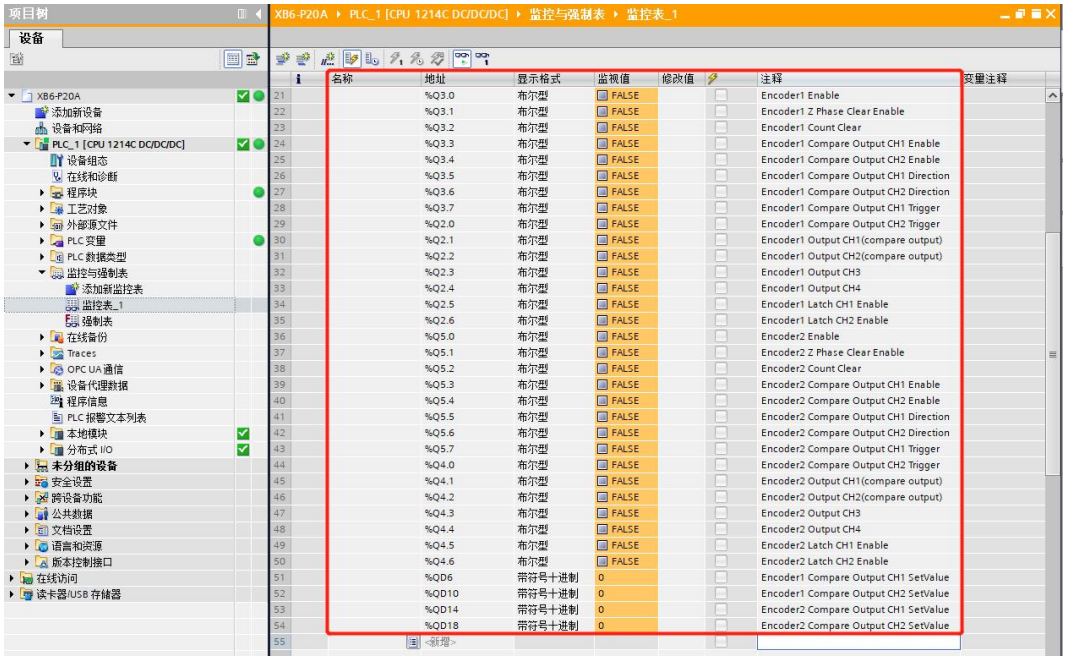
The correspondence between input and output data and addresses can be viewed through the table "XB6-P20A Variable Address Calculation Tool.xlsx".

e. The module's upstream data is shown in the monitoring table as shown below.



	名称	地址	显示格式	监视值	修改值	注释	变量注释
1		%I3.0	布尔型	FALSE		Encoder1 Latch Signal CH1	
2		%I3.1	布尔型	FALSE		Encoder1 Latch Signal CH2	
3		%I3.2	布尔型	FALSE		Encoder1 Input CH3	
4		%I3.3	布尔型	FALSE		Encoder1 Input CH4	
5		%I3.4	布尔型	FALSE		Encoder1 Latch Finish Flag CH1	
6		%I3.5	布尔型	FALSE		Encoder1 Latch Finish Flag CH2	
7		%I3.6	布尔型	FALSE		Encoder2 Latch Signal CH1	
8		%I3.7	布尔型	FALSE		Encoder2 Latch Signal CH2	
9		%I2.0	布尔型	FALSE		Encoder2 Input CH3	
10		%I2.1	布尔型	FALSE		Encoder2 Input CH4	
11		%I2.2	布尔型	FALSE		Encoder2 Latch Finish Flag CH1	
12		%I2.3	布尔型	FALSE		Encoder2 Latch Finish Flag CH2	
13		%ID4	带符号十进制	0		Encoder1 Count Value	
14		%ID8	带符号十进制	0		Encoder1 Latch Value CH1	
15		%ID12	带符号十进制	0		Encoder1 Latch Value CH2	
16		%ID16	带符号十进制	0		Encoder1 Speed	
17		%ID20	带符号十进制	0		Encoder2 Count Value	
18		%ID24	带符号十进制	0		Encoder2 Latch Value CH1	
19		%ID28	带符号十进制	0		Encoder2 Latch Value CH2	
20		%ID32	带符号十进制	0		Encoder2 Speed	
21		%Q3.0	布尔型	FALSE		Encoder1 Enable	
22		%Q3.1	布尔型	FALSE		Encoder1 Z Phase Clear Enable	
23		%Q3.2	布尔型	FALSE		Encoder1 Count Clear	
24		%Q3.3	布尔型	FALSE		Encoder1 Compare Output CH1 Enable	
25		%Q3.4	布尔型	FALSE		Encoder1 Compare Output CH2 Enable	
26		%Q3.5	布尔型	FALSE		Encoder1 Compare Output CH1 Direction	
27		%Q3.6	布尔型	FALSE		Encoder1 Compare Output CH2 Direction	
28		%Q3.7	布尔型	FALSE		Encoder1 Compare Output CH1 Trigger	
29		%Q2.0	布尔型	FALSE		Encoder1 Compare Output CH2 Trigger	
30		%Q2.1	布尔型	FALSE		Encoder1 Output CH1(compare output)	
31		%Q2.2	布尔型	FALSE		Encoder1 Output CH2(compare output)	
32		%Q2.3	布尔型	FALSE		Encoder1 Output CH3	
33		%Q2.4	布尔型	FALSE		Encoder1 Output CH4	
34		%Q2.5	布尔型	FALSE		Encoder1 Latch CH1 Enable	
35		%Q2.6	布尔型	FALSE		Encoder1 Latch CH2 Enable	
36		%Q5.0	布尔型	FALSE		Encoder2 Enable	
37		%Q5.1	布尔型	FALSE		Encoder2 Z Phase Clear Enable	
38		%Q5.2	布尔型	FALSE		Encoder2 Count Clear	
39		%Q5.3	布尔型	FALSE		Encoder2 Compare Output CH1 Enable	

f. The module's downstream data is shown in the monitoring table as shown below.



Module Functionality Examples

- **Encoder 1 inputs AB quadrature pulses, the number of pulses is 40,000, and encoder 1 probe input channel 1 is latched**

a. Configure the configuration parameters as shown in the following figure.

a) The encoder 1 pulse mode is set to AB quadrature pulse mode, that is, Encoder1 Pulse Mode is set to 0: ABZ;

b) The encoder 1 count multiple is set to 4 times, that is, Encoder1 Count Multiples is set to 4;

c) The encoder 1 count range is set to 0~ring count resolution×count multiples-1, that is, Encoder1 Count Range is set to 1: Resolution×Multiples;

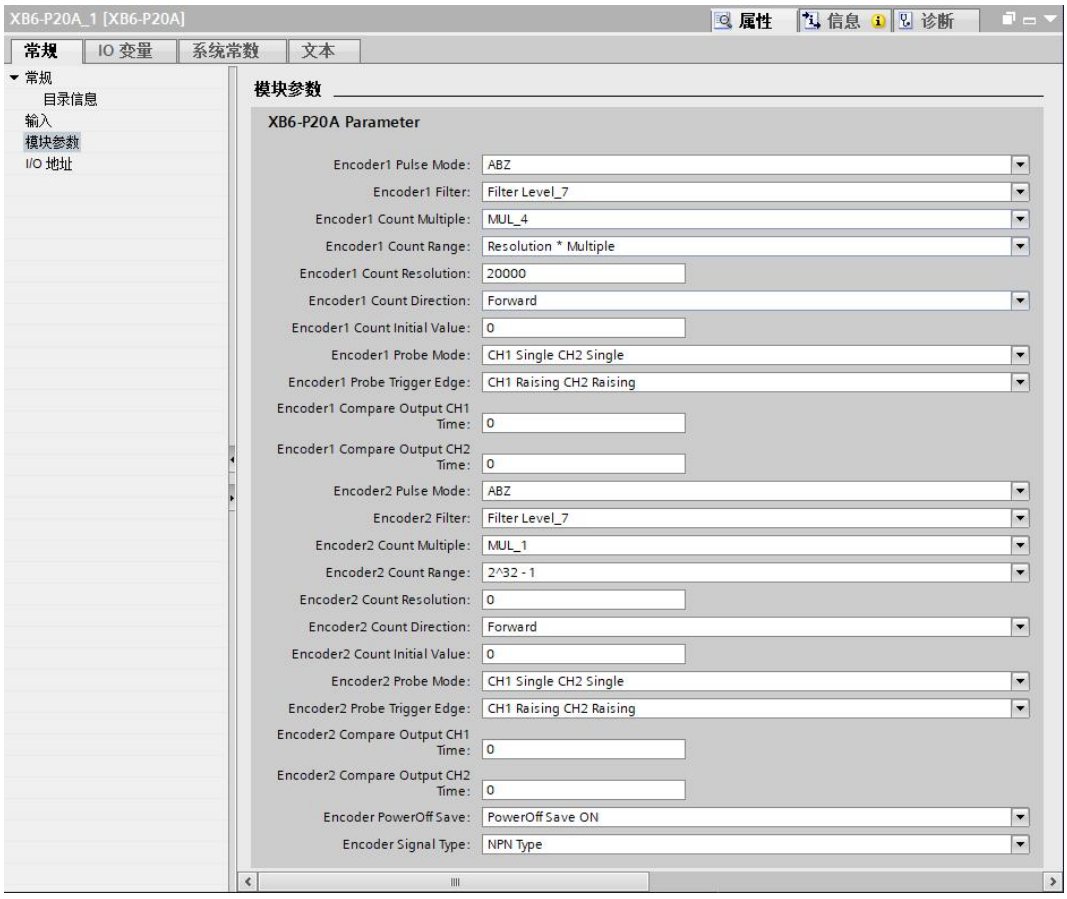
d) The encoder 1 ring count resolution is set to 20000, that is, Encoder1 Count Resolution is set to 20000;

e) The encoder 1 counting direction is set to forward counting, that is, Encoder1 Count Direction is set to 0: Forward;

f) The initial value of encoder 1 count is set to 0, that is, Encoder1 Count Initial Value is set to 0;

g) The probe mode of encoder 1 is set to single for channel 1 and single for channel 2, that is, Encoder1 Probe Trigger Mode is set to 0: CH1_Single CH2_Single;

h) The encoder 1 probe trigger edge is set to the rising edge of channel 1 and the rising edge of channel 2, that is, Encoder1 Probe Trigger Edge is set to 0: CH1_Raising CH2_Raising.

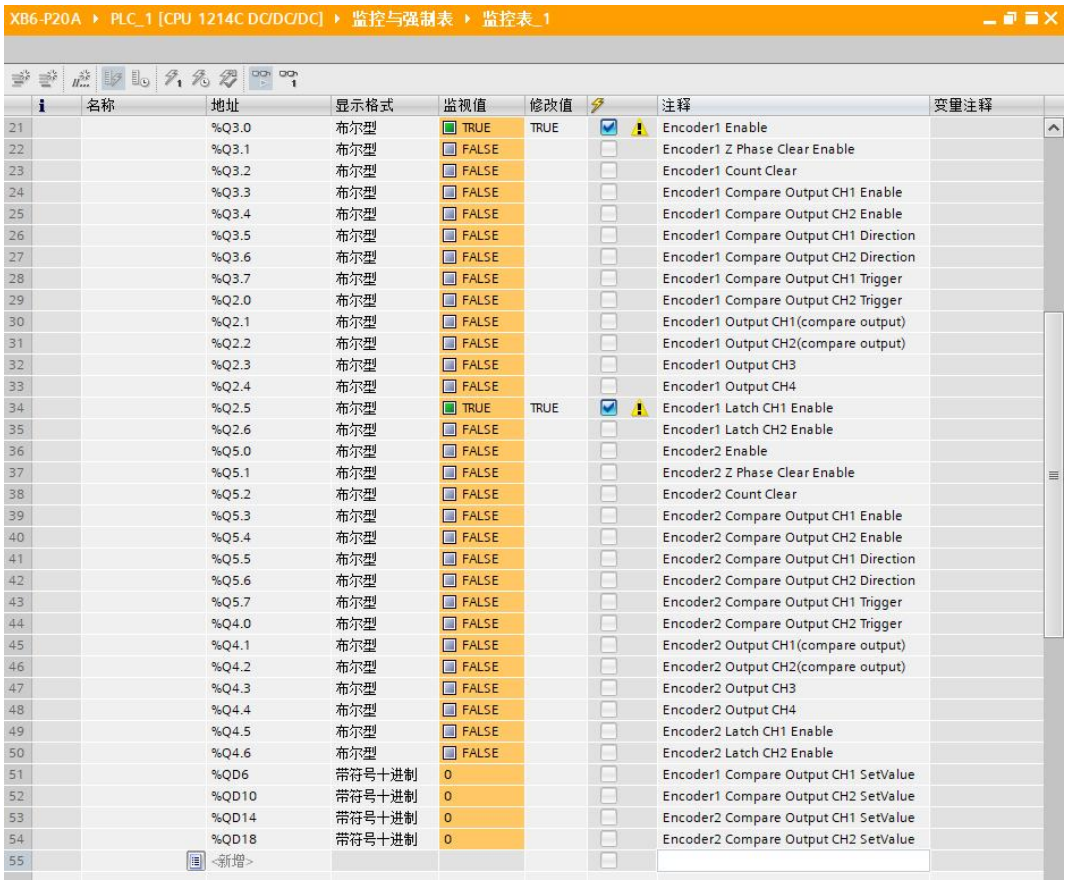


After the parameter configuration is completed, the program needs to be downloaded to the PLC again, and the PLC and the module need to be powered on again.

b. Set encoder 1 count enable and encoder 1 probe input channel 1 latch enable, as shown in the figure below.

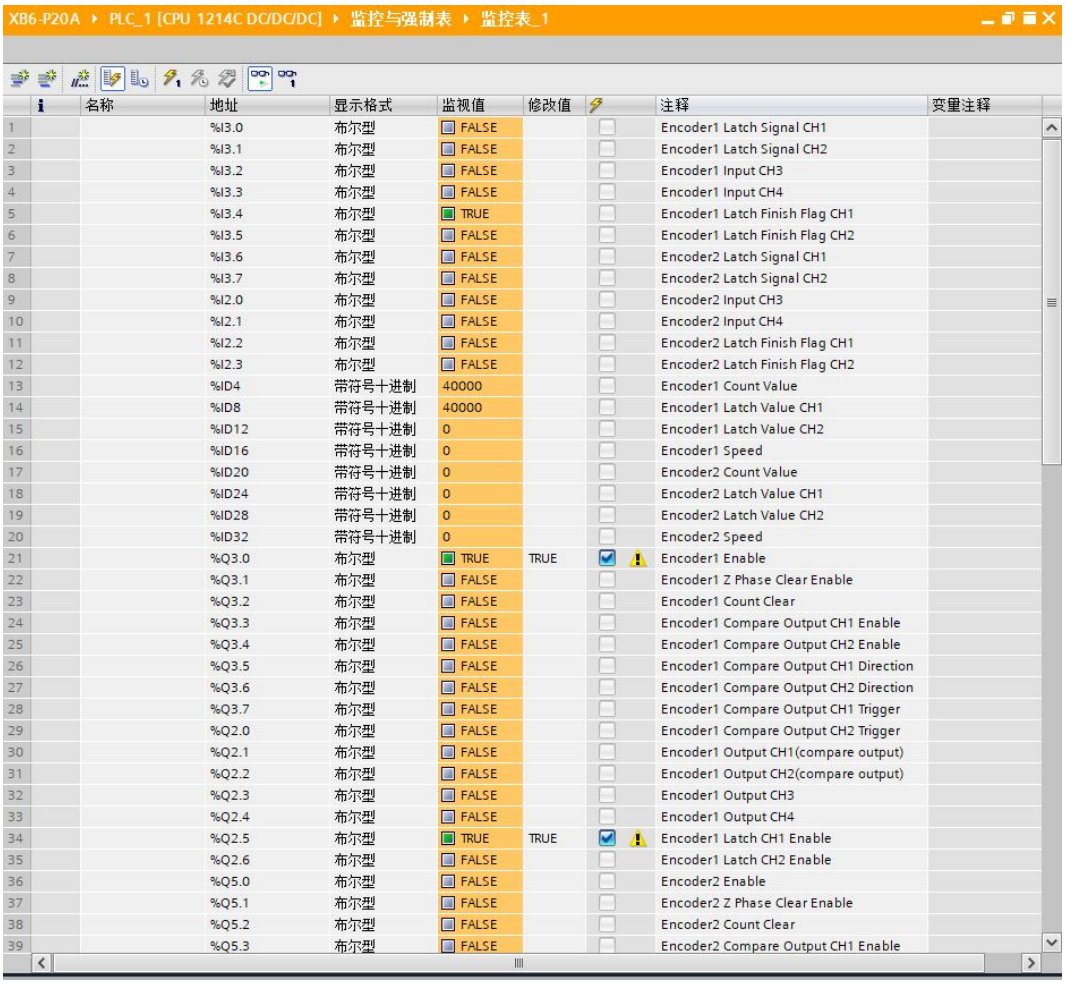
a) Downlink data Encoder_1 Enable is set to 1;

b) Set the downstream data Encoder_1 Input Latch CH1 Enable to 1.



	名称	地址	显示格式	监视值	修改值	注释	变量注释
21		%Q3.0	布尔型	TRUE	TRUE	Encoder1 Enable	
22		%Q3.1	布尔型	FALSE		Encoder1 Z Phase Clear Enable	
23		%Q3.2	布尔型	FALSE		Encoder1 Count Clear	
24		%Q3.3	布尔型	FALSE		Encoder1 Compare Output CH1 Enable	
25		%Q3.4	布尔型	FALSE		Encoder1 Compare Output CH2 Enable	
26		%Q3.5	布尔型	FALSE		Encoder1 Compare Output CH1 Direction	
27		%Q3.6	布尔型	FALSE		Encoder1 Compare Output CH2 Direction	
28		%Q3.7	布尔型	FALSE		Encoder1 Compare Output CH1 Trigger	
29		%Q2.0	布尔型	FALSE		Encoder1 Compare Output CH2 Trigger	
30		%Q2.1	布尔型	FALSE		Encoder1 Output CH1(compare output)	
31		%Q2.2	布尔型	FALSE		Encoder1 Output CH2(compare output)	
32		%Q2.3	布尔型	FALSE		Encoder1 Output CH3	
33		%Q2.4	布尔型	FALSE		Encoder1 Output CH4	
34		%Q2.5	布尔型	TRUE	TRUE	Encoder1 Latch CH1 Enable	
35		%Q2.6	布尔型	FALSE		Encoder1 Latch CH2 Enable	
36		%Q5.0	布尔型	FALSE		Encoder2 Enable	
37		%Q5.1	布尔型	FALSE		Encoder2 Z Phase Clear Enable	
38		%Q5.2	布尔型	FALSE		Encoder2 Count Clear	
39		%Q5.3	布尔型	FALSE		Encoder2 Compare Output CH1 Enable	
40		%Q5.4	布尔型	FALSE		Encoder2 Compare Output CH2 Enable	
41		%Q5.5	布尔型	FALSE		Encoder2 Compare Output CH1 Direction	
42		%Q5.6	布尔型	FALSE		Encoder2 Compare Output CH2 Direction	
43		%Q5.7	布尔型	FALSE		Encoder2 Compare Output CH1 Trigger	
44		%Q4.0	布尔型	FALSE		Encoder2 Compare Output CH2 Trigger	
45		%Q4.1	布尔型	FALSE		Encoder2 Output CH1(compare output)	
46		%Q4.2	布尔型	FALSE		Encoder2 Output CH2(compare output)	
47		%Q4.3	布尔型	FALSE		Encoder2 Output CH3	
48		%Q4.4	布尔型	FALSE		Encoder2 Output CH4	
49		%Q4.5	布尔型	FALSE		Encoder2 Latch CH1 Enable	
50		%Q4.6	布尔型	FALSE		Encoder2 Latch CH2 Enable	
51		%QD6	带符号十进制	0		Encoder1 Compare Output CH1 SetValue	
52		%QD10	带符号十进制	0		Encoder1 Compare Output CH2 SetValue	
53		%QD14	带符号十进制	0		Encoder2 Compare Output CH1 SetValue	
54		%QD18	带符号十进制	0		Encoder2 Compare Output CH2 SetValue	
55	<新增>						

c. Encoder 1 starts to input 40,000 pulses. After the pulse counting is completed, encoder 1 probe input channel 1 inputs a valid signal, the encoder 1 count value is 40,000, the probe input channel 1 latch value is 40,000, and the encoder probe input channel 1 latch completion flag value flips once to 1, as shown in the figure below.



	名称	地址	显示格式	监视值	修改值	注释	变量注释
1		%I3.0	布尔型	FALSE		Encoder1 Latch Signal CH1	
2		%I3.1	布尔型	FALSE		Encoder1 Latch Signal CH2	
3		%I3.2	布尔型	FALSE		Encoder1 Input CH3	
4		%I3.3	布尔型	FALSE		Encoder1 Input CH4	
5		%I3.4	布尔型	TRUE		Encoder1 Latch Finish Flag CH1	
6		%I3.5	布尔型	FALSE		Encoder1 Latch Finish Flag CH2	
7		%I3.6	布尔型	FALSE		Encoder2 Latch Signal CH1	
8		%I3.7	布尔型	FALSE		Encoder2 Latch Signal CH2	
9		%I2.0	布尔型	FALSE		Encoder2 Input CH3	
10		%I2.1	布尔型	FALSE		Encoder2 Input CH4	
11		%I2.2	布尔型	FALSE		Encoder2 Latch Finish Flag CH1	
12		%I2.3	布尔型	FALSE		Encoder2 Latch Finish Flag CH2	
13		%ID4	带符号十进制	40000		Encoder1 Count Value	
14		%ID8	带符号十进制	40000		Encoder1 Latch Value CH1	
15		%ID12	带符号十进制	0		Encoder1 Latch Value CH2	
16		%ID16	带符号十进制	0		Encoder1 Speed	
17		%ID20	带符号十进制	0		Encoder2 Count Value	
18		%ID24	带符号十进制	0		Encoder2 Latch Value CH1	
19		%ID28	带符号十进制	0		Encoder2 Latch Value CH2	
20		%ID32	带符号十进制	0		Encoder2 Speed	
21		%Q3.0	布尔型	TRUE	TRUE	Encoder1 Enable	
22		%Q3.1	布尔型	FALSE		Encoder1 Z Phase Clear Enable	
23		%Q3.2	布尔型	FALSE		Encoder1 Count Clear	
24		%Q3.3	布尔型	FALSE		Encoder1 Compare Output CH1 Enable	
25		%Q3.4	布尔型	FALSE		Encoder1 Compare Output CH2 Enable	
26		%Q3.5	布尔型	FALSE		Encoder1 Compare Output CH1 Direction	
27		%Q3.6	布尔型	FALSE		Encoder1 Compare Output CH2 Direction	
28		%Q3.7	布尔型	FALSE		Encoder1 Compare Output CH1 Trigger	
29		%Q2.0	布尔型	FALSE		Encoder1 Compare Output CH2 Trigger	
30		%Q2.1	布尔型	FALSE		Encoder1 Output CH1(compare output)	
31		%Q2.2	布尔型	FALSE		Encoder1 Output CH2(compare output)	
32		%Q2.3	布尔型	FALSE		Encoder1 Output CH3	
33		%Q2.4	布尔型	FALSE		Encoder1 Output CH4	
34		%Q2.5	布尔型	TRUE	TRUE	Encoder1 Latch CH1 Enable	
35		%Q2.6	布尔型	FALSE		Encoder1 Latch CH2 Enable	
36		%Q5.0	布尔型	FALSE		Encoder2 Enable	
37		%Q5.1	布尔型	FALSE		Encoder2 Z Phase Clear Enable	
38		%Q5.2	布尔型	FALSE		Encoder2 Count Clear	
39		%Q5.3	布尔型	FALSE		Encoder2 Compare Output CH1 Enable	

- **Encoder 1 input direction pulse, pulse quantity 40000, encoder 1 comparison output channel 1 comparison output**

a. Configure the configuration parameters as shown in the following figure.

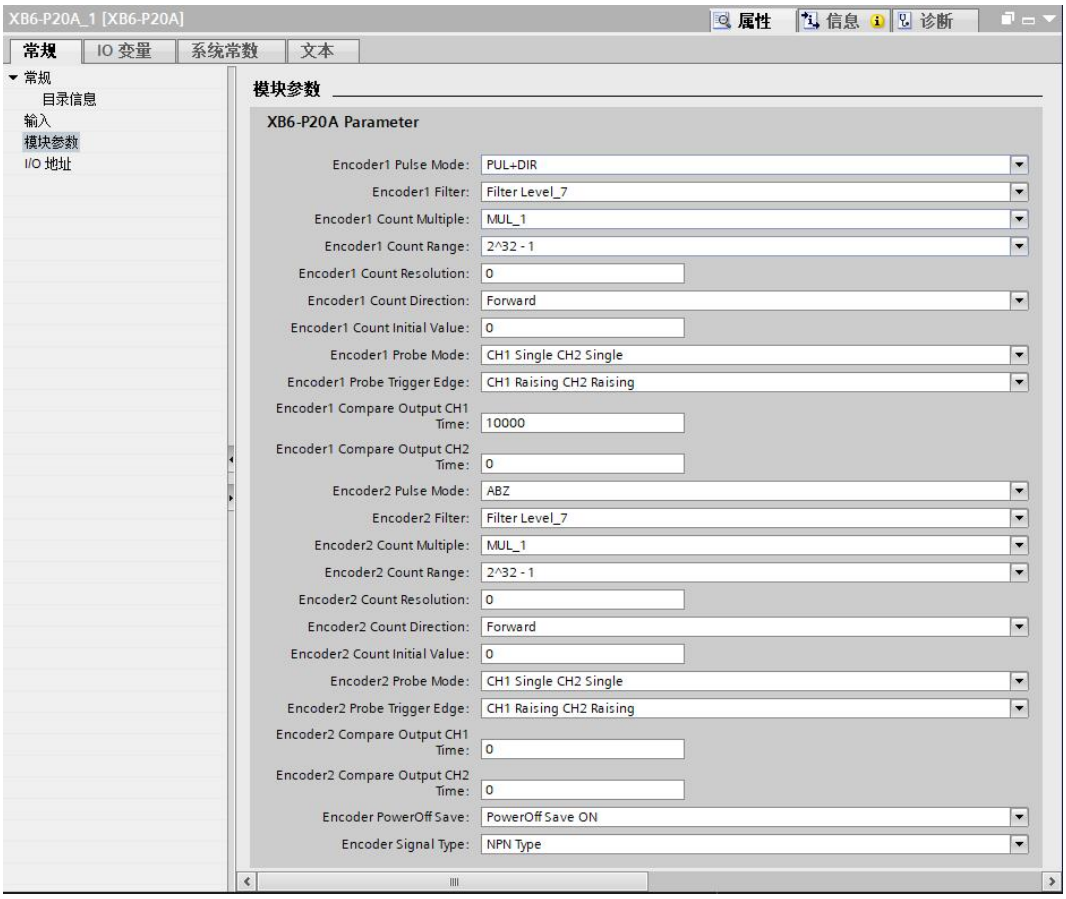
a) The encoder 1 pulse mode is set to the direction pulse mode, that is, Encoder1 Pulse Mode is set to 1: Pul+Dir;

b) The encoder 1 count range is set to 0~2^32-1, that is, Encoder1 Count Range is set to 0:2^32;

c) The encoder 1 counting direction is set to forward counting, that is, Encoder1 Count Direction is set to 0: Forward;

d) The initial value of encoder 1 count is set to 0, that is, Encoder1 Count Initial Value is set to 0;

e) The encoder 1 compare output channel 1 pulse time is set to 10s, that is, Encoder1 Compare Output CH1 Time is set to 10000.



After the parameter configuration is completed, the program needs to be downloaded to the PLC again, and the PLC and the module need to be powered on again.

b. Set encoder 1 counting enable, encoder 1 comparison output channel 1 set comparison set value, comparison direction and comparison mode and enable, as shown in the following figure.

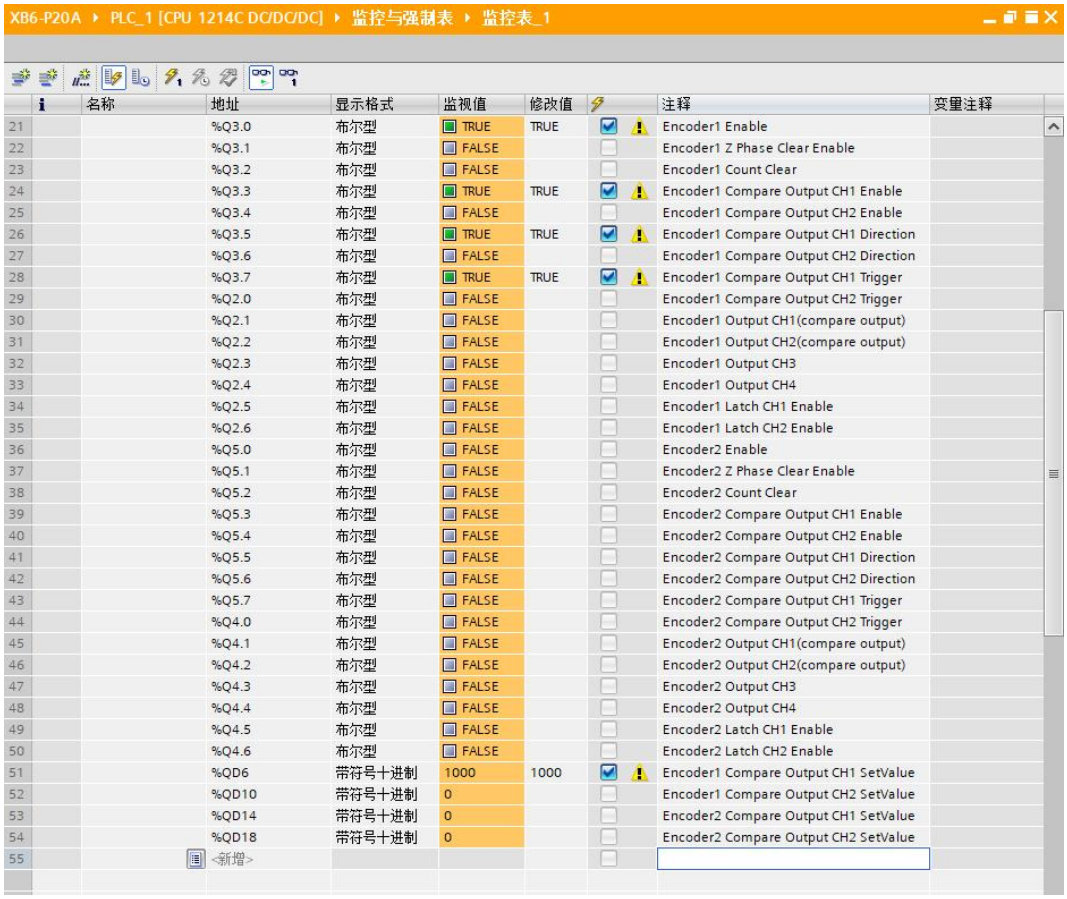
a) Downlink data Encoder_1 Enable is set to 1;

b) Downlink data Encoder_1 Compare Output CH1 SetValue is set to 1000;

c) Downlink data Encoder_1 Compare Output CH1 Direction is set to 1 for incremental comparison;

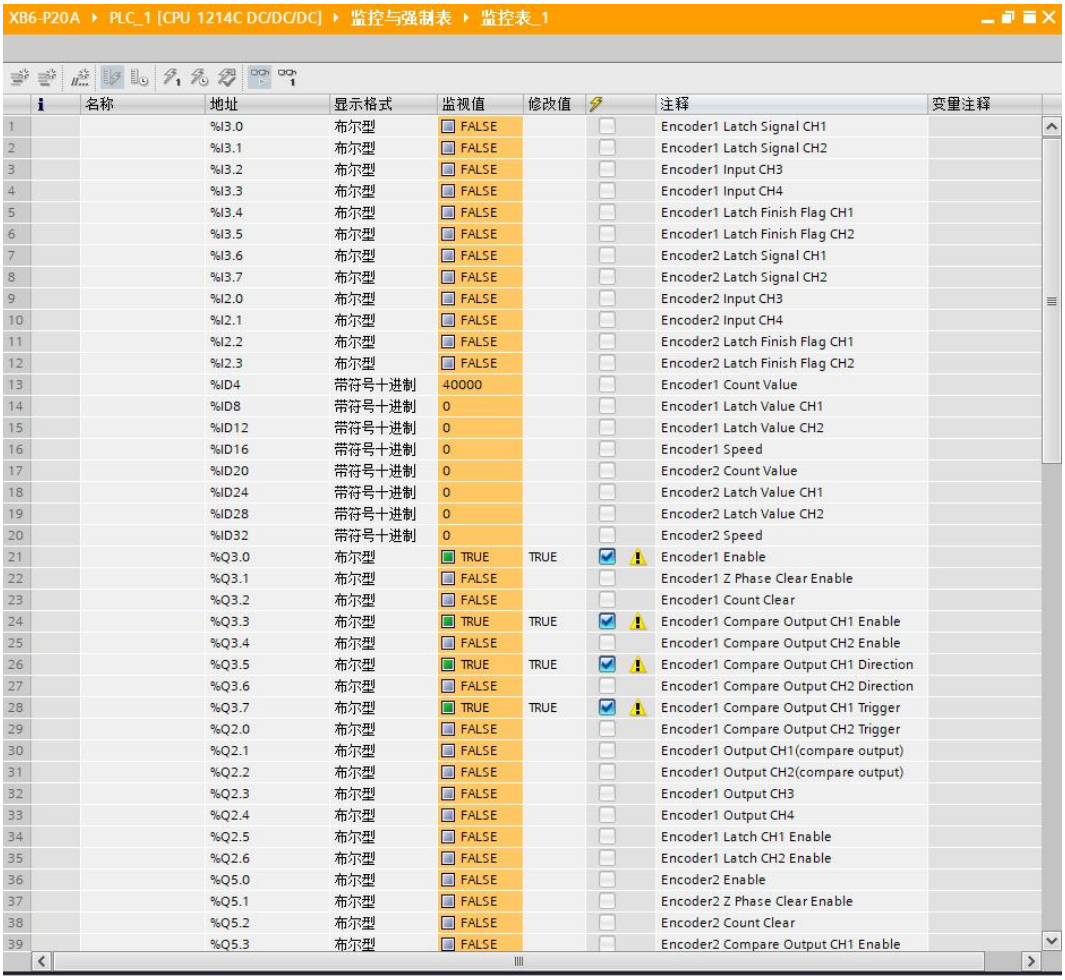
d) Downlink data Encoder_1 Compare Output CH1 Mode is set to 1 Repeat Trigger;

e) Set the downstream data Encoder_1 Compare Output CH1 Enable to 1 to enable.



	名称	地址	显示格式	监视值	修改值	注释	变量注释
21		%Q3.0	布尔型	TRUE	TRUE	Encoder1 Enable	
22		%Q3.1	布尔型	FALSE		Encoder1 Z Phase Clear Enable	
23		%Q3.2	布尔型	FALSE		Encoder1 Count Clear	
24		%Q3.3	布尔型	TRUE	TRUE	Encoder1 Compare Output CH1 Enable	
25		%Q3.4	布尔型	FALSE		Encoder1 Compare Output CH2 Enable	
26		%Q3.5	布尔型	TRUE	TRUE	Encoder1 Compare Output CH1 Direction	
27		%Q3.6	布尔型	FALSE		Encoder1 Compare Output CH2 Direction	
28		%Q3.7	布尔型	TRUE	TRUE	Encoder1 Compare Output CH1 Trigger	
29		%Q2.0	布尔型	FALSE		Encoder1 Compare Output CH2 Trigger	
30		%Q2.1	布尔型	FALSE		Encoder1 Output CH1(compare output)	
31		%Q2.2	布尔型	FALSE		Encoder1 Output CH2(compare output)	
32		%Q2.3	布尔型	FALSE		Encoder1 Output CH3	
33		%Q2.4	布尔型	FALSE		Encoder1 Output CH4	
34		%Q2.5	布尔型	FALSE		Encoder1 Latch CH1 Enable	
35		%Q2.6	布尔型	FALSE		Encoder1 Latch CH2 Enable	
36		%Q5.0	布尔型	FALSE		Encoder2 Enable	
37		%Q5.1	布尔型	FALSE		Encoder2 Z Phase Clear Enable	
38		%Q5.2	布尔型	FALSE		Encoder2 Count Clear	
39		%Q5.3	布尔型	FALSE		Encoder2 Compare Output CH1 Enable	
40		%Q5.4	布尔型	FALSE		Encoder2 Compare Output CH2 Enable	
41		%Q5.5	布尔型	FALSE		Encoder2 Compare Output CH1 Direction	
42		%Q5.6	布尔型	FALSE		Encoder2 Compare Output CH2 Direction	
43		%Q5.7	布尔型	FALSE		Encoder2 Compare Output CH1 Trigger	
44		%Q4.0	布尔型	FALSE		Encoder2 Compare Output CH2 Trigger	
45		%Q4.1	布尔型	FALSE		Encoder2 Output CH1(compare output)	
46		%Q4.2	布尔型	FALSE		Encoder2 Output CH2(compare output)	
47		%Q4.3	布尔型	FALSE		Encoder2 Output CH3	
48		%Q4.4	布尔型	FALSE		Encoder2 Output CH4	
49		%Q4.5	布尔型	FALSE		Encoder2 Latch CH1 Enable	
50		%Q4.6	布尔型	FALSE		Encoder2 Latch CH2 Enable	
51		%QD6	带符号十进制	1000	1000	Encoder1 Compare Output CH1 SetValue	
52		%QD10	带符号十进制	0		Encoder1 Compare Output CH2 SetValue	
53		%QD14	带符号十进制	0		Encoder2 Compare Output CH1 SetValue	
54		%QD18	带符号十进制	0		Encoder2 Compare Output CH2 SetValue	
55		<新增>					

c. Encoder 1 starts to input 40,000 pulses. The count value goes up from 0. When it reaches 1,000 (satisfying the comparison setting value and direction), the comparison output channel 1 state flips from the original low-level output to high-level output. The pulse output time is 10s, and the channel indicator light will be on for 10s. After the counting is completed, the encoder 1 count value is 40,000, as shown in the figure below.



	名称	地址	显示格式	监视值	修改值		注释	变量注释
1		%I3.0	布尔型	FALSE			Encoder1 Latch Signal CH1	
2		%I3.1	布尔型	FALSE			Encoder1 Latch Signal CH2	
3		%I3.2	布尔型	FALSE			Encoder1 Input CH3	
4		%I3.3	布尔型	FALSE			Encoder1 Input CH4	
5		%I3.4	布尔型	FALSE			Encoder1 Latch Finish Flag CH1	
6		%I3.5	布尔型	FALSE			Encoder1 Latch Finish Flag CH2	
7		%I3.6	布尔型	FALSE			Encoder2 Latch Signal CH1	
8		%I3.7	布尔型	FALSE			Encoder2 Latch Signal CH2	
9		%I2.0	布尔型	FALSE			Encoder2 Input CH3	
10		%I2.1	布尔型	FALSE			Encoder2 Input CH4	
11		%I2.2	布尔型	FALSE			Encoder2 Latch Finish Flag CH1	
12		%I2.3	布尔型	FALSE			Encoder2 Latch Finish Flag CH2	
13		%ID4	带符号十进制	40000			Encoder1 Count Value	
14		%ID8	带符号十进制	0			Encoder1 Latch Value CH1	
15		%ID12	带符号十进制	0			Encoder1 Latch Value CH2	
16		%ID16	带符号十进制	0			Encoder1 Speed	
17		%ID20	带符号十进制	0			Encoder2 Count Value	
18		%ID24	带符号十进制	0			Encoder2 Latch Value CH1	
19		%ID28	带符号十进制	0			Encoder2 Latch Value CH2	
20		%ID32	带符号十进制	0			Encoder2 Speed	
21		%Q3.0	布尔型	TRUE	TRUE		Encoder1 Enable	
22		%Q3.1	布尔型	FALSE			Encoder1 Z Phase Clear Enable	
23		%Q3.2	布尔型	FALSE			Encoder1 Count Clear	
24		%Q3.3	布尔型	TRUE	TRUE		Encoder1 Compare Output CH1 Enable	
25		%Q3.4	布尔型	FALSE			Encoder1 Compare Output CH2 Enable	
26		%Q3.5	布尔型	TRUE	TRUE		Encoder1 Compare Output CH1 Direction	
27		%Q3.6	布尔型	FALSE			Encoder1 Compare Output CH2 Direction	
28		%Q3.7	布尔型	TRUE	TRUE		Encoder1 Compare Output CH1 Trigger	
29		%Q2.0	布尔型	FALSE			Encoder1 Compare Output CH2 Trigger	
30		%Q2.1	布尔型	FALSE			Encoder1 Output CH1(compare output)	
31		%Q2.2	布尔型	FALSE			Encoder1 Output CH2(compare output)	
32		%Q2.3	布尔型	FALSE			Encoder1 Output CH3	
33		%Q2.4	布尔型	FALSE			Encoder1 Output CH4	
34		%Q2.5	布尔型	FALSE			Encoder1 Latch CH1 Enable	
35		%Q2.6	布尔型	FALSE			Encoder1 Latch CH2 Enable	
36		%Q5.0	布尔型	FALSE			Encoder2 Enable	
37		%Q5.1	布尔型	FALSE			Encoder2 Z Phase Clear Enable	
38		%Q5.2	布尔型	FALSE			Encoder2 Count Clear	
39		%Q5.3	布尔型	FALSE			Encoder2 Compare Output CH1 Enable	